Appeal decision

Appeal No. 2014-6575

USA
Appellant SUNPOWER CORPORATION

Tokyo, Japan
Patent Attorney RYUKA IP LAW FIRM

The appeal case against the examiner's refusal decision regarding Japanese Patent Application No. 2010-510284, entitled "Array of small contacts for solar cell fabrication" [International publication: WO 2008/150344, Dec. 11, 2008; Domestic publication of PCT Application: No. 2010-528487, Aug. 19, 2010, the number of claims: 10] has resulted in the following conclusion.

Conclusion

The examiner's decision is revoked.

The invention of the present application shall be granted a patent.

Reason

No. 1 History of the procedures

The application was originally filed on May 12, 2008 as an International Patent Application (Priority claim under the Paris Convention*:* May 29, 2007, US), an amendment was submitted on May 9, 2011, a notification of reasons for refusal was issued on Dec. 28, 2012, an written argument and an written amendment were submitted on Apr. 8, 2013, a final notification of reasons of refusal was issued on Jul. 12, 2013, and an written argument and an written amendment were submitted on Oct. 16, 2013.

As a result, the decision to dismiss the written amendment dated Oct. 16, 2013 was issued on Dec. 6, 2013 and at the same time the refusal decision was issued on the same day.

The appeal against the refusal decision was filed on Apr. 9, 2014 and at the same time a written amendment was submitted.

An examiner's reconsideration report to the JPO Commissioner was issued on

Jun. 25, 2014 prior to the appeal proceeding.

1. Notification of reasons for refusal dated Jul. 12, 2013

The reasons for refusal, which were notified and grounds for the decision for refusal, dated Jul. 12, 2013 (hereinafter, simply referred to as "Reasons for Refusal") are as follows.

Reasons

(Reason 1)

The statements of claims of the application fail to fulfill the requirements stipulated in Article 36(6)(ii) of the Patent Act from the following viewpoints.

Details

As for the invention according to claim 1, it contains unclear matters.

Claim 1 contains a description "by inkjet printing of a plurality of dots at least to an opening between the second dielectric layers, gaps are formed by intersections of the dots, where the interval of the gaps are specified by an arrangement of inkjet printer nozzles that supply the dots and a size of the dots."

However, in the light of common general technical knowledge as of the moment when the application was filed, as for inkjet printing coating by means of a plurality of nozzles, not all the nozzles but selected ones are used on a certain printing. Therefore, the size of a gap formed by intersections of dots depends on the nozzles that are selected and used for printing (if necessary, refer to FIG. 13A, FIG. 13B, FIG. 24, FIG. 26, etc. of Japanese Unexamined Patent Application Publication No. 2004-209887).

Since the interval of gaps is related to an arrangement of nozzles and the size of dots and further it can change significantly according to nozzles selectively used, it is thought that the interval of gaps doesn't depend on an arrangement of nozzles, which create dots, in conjunction with the size of the dots.

Consequently, the invention according to claim 1 remains unclear since it states that the interval of gaps of dots is determined by an arrangement of inkjet nozzles that create dots in conjunction with the size of the dots.

The same thing is applied to claims 2 to 7, which are dependent on claim 1.

(Reason 2)

The inventions according to the following claims of this application could have been invented easily by a person skilled in the art in the field of the technology to which the inventions belong based on inventions disclosed in the following Publications that has been distributed prior to the filing of the application in Japan or a foreign country or on inventions that had been made publicly available through an electric telecommunication line prior to the filing of the application in Japan or a foreign country, and, thus, the appellant should not be granted a patent for these in accordance with the provisions of Article 29(2) of the Patent Act.

(See below regarding Cited Documents etc.)

- Claims 1, 3, and 4
- Cited Documents 1 and 2

Notes:

Cited Document 1 shows that a solar cell in which: a dielectric layer made of SiO2 and the like is formed between an n-doped region and a p-doped region provided on the back face of a silicon substrate such that openings corresponding to the n-doped region and the p-doped region are provided; electrodes of each conductivity type are formed in the openings; and an insulation layer made of polyimide is formed to insulate the electrodes of each conductivity type from each other (especially, refer to [0049] to [0061], [0077], [FIG. 6], [FIG. 7], and [FIG. 12]).

Cited Document 1 doesn't teach a manner that a mask is formed by an inkjet printing, a passivating layer are made of SiO2 and the like, or openings of an insulator layer of polyimide are made.

However, Cited Document 2 teaches a manner that inkjet printing method is used after forming two layers of insulation films on a semiconductor chip. It also shows that silicon oxide and polyimide are used as a material of insulation films (in particular, refer to [0059], [0082] to [0093], [FIG. 7], and [FIG. 8]).

Since both the invention shown in Cited Document 1 and that shown in Cited Document 2 belong to the same technical field of an electrode forming method for a semiconductor device with a film made of SiO2 and the like and a layer made of polyimide, so they are closely related to each other.

Therefore, it could be achieved easily by a person skilled in the art to apply the method shown in Cited Document 2 to a method of forming an opening in an insulation

film of the invention shown in Cited Document 1.

In addition, in the inkjet printing method, ink or liquid droplets are ejected from nozzles with predetermined-diameter openings arranged at a predetermined pitch, when the interval of gaps created between ink is determined on the basis of an arrangement of plural nozzles and the size of a dot, it is recognized that in inkjet printing method an interval of gaps created between ink necessarily depends on the interval of dots based on the size of dots that is caused by an arrangement of nozzles of an inkjet printing printer and some affinity between ink and media the ink is applied to.

Consequently, the inventions according to claims 1, 3, and 4 of the present application could have been easily invented by a person skilled in the art on the basis of the inventions shown in Cited Documents 1 and 2.

- Claim 2
- Cited Documents 1 to 4

Notes:

Since a forming method of an insulation layer is unclear in the Cited Document 1, screen printing is a well-known forming method for making an insulation layer made of polyimide to a person skilled in the art (refer to Cited Documents 3 and 4), it could have been easily achieved by a person skilled in the art to employ a well-known screen printing for making a polyimide insulation layer in the invention shown in Cited Document 1.

- Claims 5, and 8 to 10
- Cited Documents 1 to 4

Notes:

Since an area on which an insulation layer is provided can be selected by a person skilled in the art as long as the insulation works electrically between electrodes in accordance with types of a semiconductor device and various attributes needed for the semiconductor device, a person skilled in the art could easily make an insulation layer made of polyimide over a part of an N-type layer in the invention shown in Cited Document 1 to derive the inventions according to claims 5, and 8 to 10 of the present application.

- Claims 6, 7
- Cited Documents 1 to 6

Notes:

It is commonly conducted for inkjet printing at the time of filing of the present application to perform printing on one printing area with overlapping ink in a single pass and perform printing with overlapping ink in multiple passes (refer to the Cited Documents 5, 6). A person skilled in the art can determine the number of passes to perform printing according to printing speed, printing precision and the like.

Therefore, a person skilled in the art could easily set the number of the passes in the invention described in the Cited Document 1 to derive the inventions according to claims 6 and 7 of the present application.

List of Cited Documents and the like

1. Japanese Unexamined Patent Application Publication No. 2001-189482
2. Japanese Unexamined Patent Application Publication No. 2002-158248
3. Japanese Unexamined Patent Application Publication No. 2006-261089
4. Japanese Unexamined Patent Application Publication No. 2003-298078
5. Japanese Unexamined Patent Application Publication No. 2007-125855
6. Japanese Unexamined Patent Application Publication No. H11-138787

"

2. Details of the decision of refusal dated Dec. 6, 2013

The details of the decision of refusal dated Dec. 6, 2013 (hereinafter, simply referred to as "Decision of Refusal") are as follows.

"

This application should be rejected based on the reason described in the written notice of reasons for refusal dated Jul. 12, 2013.

Meanwhile, although the contents of the written opinion were examined, sufficient grounds for overturning the reason for refusal were not found.

Notes

The written amendment dated Oct. 16, 2013 was dismissed at the same time with this examiner's decision,

"

3. Detail of the reconsideration report made to the JPO Commissioner in the procedure of reconsideration by examiners before appeal proceedings dated Jun. 25, 2014

The details of the reconsideration report made to the JPO Commissioner in the procedure of reconsideration by examiners before appeal proceedings dated Jun. 25, 2014 (hereinafter, just referred to as "Reconsideration Report") are as follows.

"

Regarding the application relating to this demand for appeal, a report will be made as follows.

Details

Details (See below regarding Cited Documents etc)

The purpose of the amendment as to claim 1 is to restrict the scope of the claim. In this case, the invention according to claim 1 after amendment must be one which should be independently patentable at the time of the patent application.

However, since it was well-known as of the moment when the application was filed to form a mask pattern with openings by means of inkjet printing and etching of desired areas (refer to Cited Documents 2, 3), it would have been easy for a person skilled in the art to adopt the well-known method for forming a penetration hole of an insulation film in the invention shown in Cited Document 1.

In addition, since it is obvious for a person skilled in the art that an opening with the size depending on the interval of nozzles of an inkjet printing printer and a dot diameter of ink is formed where the ink is not ejected, from the drawings and the like of Cited Document 4 ([FIG. 13], [FIG. 24], [FIG. 26]), it could have been achieved by a person skilled in the art to determine a dot diameter of ink and whether or not to eject ink based on the size of an opening, an opening-formed area, and a nozzle pitch of heads of an inkjet printer in order to obtain a desired opening.

Accordingly, the appellant should not be granted a patent independently according to claim 1 after the amendment at the time of the patent application under the provisions of Article 29(2) of the Patent Act.

In addition, also regarding claims 3 and 4 after amendment, those could have

easily been invented by a person skilled in the art from the invention shown in Cited Documents 1 to 4, and, therefore, for those the appellant should not be granted a patent independently at the time of patent application under the provisions of Article 29(2) of the Patent Act.

Regarding the inventions according to claims 2, 5, 8 to 10, claims 6 and 7 after amendment, since they could have easily been invented by a person skilled in the art on the basis of the invention shown in Cited Documents 1 to 6, and that shown in Cited Documents 1 to 8, respectively, the appellant should not be granted a patent independently for these inventions at the time of patent application under the provisions of Article 29(2) of the Patent Act.

Therefore, this amendment violates the provisions of Article 126(7) of the Patent Act as applied mutatis mutandis pursuant to the provisions of Article 17-2(6) of the Patent Act, and, therefore, it should be dismissed under the provisions of Article 53(1) of the Patent Act as applied mutatis mutandis pursuant to the provisions of Article 159(1) of the Patent Act with relevant changes in interpretation.

Therefore, this application should be rejected as indicated in the reason of the examiner's decision.

List of the Cited Documents, etc.

1. Japanese Unexamined Patent Application Publication No. 2001-189482
2. Japanese Unexamined Patent Application Publication No. 2002-158248
3. Japanese Unexamined Patent Application Publication No. 2006-124805
4. Japanese Unexamined Patent Application Publication No. 2004-209887
5. Japanese Unexamined Patent Application Publication No. 2006-261089
6. Japanese Unexamined Patent Application Publication No. 2003-298078
7. Japanese Unexamined Patent Application Publication No. 2007-125855
8. Japanese Unexamined Patent Application Publication No. H11-138787

"

No. 2 The Amended Invention

According to the amendment dated Apr. 9, 2014 (hereinafter, referred to as "Amendment of the case"), the scope of claims of the present application was amended for the purpose of restriction of the scope of claims prescribed in Article 17-2(5)(ii) of the Patent Act.

Therefore, the inventions according to claims 1 to 10 after the Amendment of the case

(hereinafter, referred to as "Amended Inventions 1 to 10," respectively) are described in claims 1 to 10 of the claims after the amendment of the case as follows.

" [Claim 1]

A method of fabricating a solar cell, the method comprising:

forming a first dielectric layer over a wafer to be processed into a solar cell;

forming a plurality of second dielectric layers over the first dielectric layer; and

inkjet printing a plurality of dots at least in openings between the second dielectric layers to form a plurality of gaps formed by intersections of the dots and having a smaller area than an area of the dots, a size of the gaps being dictated at least by (i) an alignment of inkjet printer nozzles that supply the plurality of dots, (ii) the size of the dots, and (iii) which nozzles are used.

[Claim 2]

The method of claim 1, wherein the second dielectric layers comprise a polyimide screen printed over the wafer.

[Claim 3]

The method of claim 1, further comprising:

forming contact regions through the first dielectric layer using the plurality of dots as a mask;

removing the plurality of dots from the wafer; and

forming metal contact fingers over the first dielectric layer to create electrical connections through the contact regions to diffusion regions under the first dielectric layer.

[Claim 4]

The method of claim 3, wherein the at least some of the metal contact fingers comprise N-type metal contact fingers formed to create electrical connections to corresponding N-type diffusion regions through at least some of the contact regions and P-type metal contact fingers formed to create electrical connections to corresponding P-type diffusion regions through at least some of the contact regions, the P-type and N-type diffusion regions being formed on a backside of the wafer, which is opposite a front side of the wafer facing the sun during normal operation.

[Claim 5]

The method of claim 4, wherein the N-type metal contact fingers but not the P-type metal contact fingers are formed over the second dielectric layers.

[Claim 6]

The method of claim 1, wherein the dots are printed in one pass of a print head including the nozzles in one direction over the wafer.

[Claim 7]

The method of claim 6, further comprising:

passing the print head over the wafer at least in another pass to print another dot covering a gap in the plurality of gaps.

[Claim 8]

A method of fabricating a solar cell, the method comprising:

forming a first dielectric layer over a solar cell wafer having diffusion regions adjacent to each other;

forming a plurality of second dielectric layers over the first dielectric layer and over boundaries between adjacent pairs of the diffusion regions;

printing a plurality of dots at least in an opening between two of the second dielectric layers, the plurality of dots forming a contact mask that forms a plurality of gaps having a smaller area than an area of the dots, each of the gaps being defined by intersections of overlapping dots in the plurality of dots; and

etching portions of the first dielectric layer exposed through the gaps to form a plurality of contact regions exposing a plurality of diffusion regions of the solar cell.

[Claim 9]

The method of claim 8, further comprising:

removing the plurality of dots from the wafer; and

forming metal contact fingers in the plurality of contact regions to electrically connect to corresponding ones in the plurality of diffusion regions.

[Claim 10]

The method of claim 8, wherein the first dielectric layer comprises silicon dioxide."

With regard to this, the Reconsideration Report states that the Amendment of the case violates the provisions of Article 126(7) of the Patent Act as applied mutatis mutandis pursuant to the provisions of Article 17-2(6) of the Patent Act, and, therefore, it should be dismissed under the provisions of Article 53(1) of the Patent Act as applied mutatis mutandis pursuant to the provisions of Article 159(1) of the Patent Act with relevant changes in interpretation since the appellant should not be granted a patent independently for the Amended Inventions 1 to 10 at the time when the patent application was filed under the provisions of Article 29(2) of the Patent Act.

Therefore, whether or not the appellant can be granted a patent independently for

the Amended Inventions 1 to 10 at the time of patent application under the provisions of Article 29(2) of the Patent Act will be taking into consideration below.

1. About Amended Invention 1

(1) Cited Document 1

Japanese Unexamined Patent application Publication No. 2001-189482 (hereinafter, referred to as "Cited Document 1"), which was cited in the Reasons for Refusal, the Decision of Refusal, and the Reconsideration Report and had been distributed before the priority date of the present application, the following matters are shown. (The underlines are added by the body.)

(a) "[0001]
[Field of the Invention] This invention relates to a method of fabricating a solar cell, and, more particularly, to a method of fabricating a back surface point contact silicon solar cell."

(b) "[0028] FIG. 2 is a process flow chart illustrating the process to a fabricate the silicon solar cell (of FIG. 1(b)) according to the present invention, and FIG. 3 and FIG. 4 are sectional views of the silicon solar cell explaining the process. Meanwhile, it should be noted here that a substrate 10 is turned bottom side up and the size and shape of a member are often deformed and overcrowded for illustration purpose in Fig. 3(a) and on.
[0029] The process begins in S10 in which, as shown in FIG. 3(a), the first passivating layer of silicon oxide 18 is formed on the silicon substrate 10, and the second passivating layer 20 made of silicon nitride is formed on the top surface of the first passivating layer 18, while the substrate 10 is formed with the passivating layer 12 at its top. Then, the opened windows 34 are formed through the first and second layers 18, 20 to expose surface portions on the substrate 10, and the phosphorus-doped glass 36 is stuck to the second layer 20 and filled into the opened windows 34.
[0030] Thereafter, processing proceeds to S12 in which, as shown in FIG. 3(b), a second plurality of opened windows 38 are pierced between the first-pierced opened windows 34 of the first group, respectively, and a boron-doped glass 40 is sticked on the surface of the substrate 10 and filled into the opened windows 38 of the second group. The structure is then heated to a temperature of approximately 900 degrees C

to 1150 degrees C, such that dopants from the doped oxide layers (glasses) 36, 40 diffuse into the surface of the substrate 10 configured as above to form the n-doped regions 14 and the p-doped region 16 mentioned above. The substrate 10 is then exposed to a silicon oxide etch to remove all of the exposed oxide layers (glasses) 36, 40 to obtain the structure illustrated in FIG. 3(c).

[0031] Meanwhile, it is supposed that, in the following description, "the substrate configured as above" means a substrate for which the processing of previous processes has been carried out.

[0032] Then, processing proceeds to S14 in which the first metal layer 24 (e.g., sputtered aluminum) is deposited over the entire surface of the second passivating layer 20 at the thickness of 2 to 4 μm to form contacts (connect electrically) with all of the n-doped regions 14 and the p-doped region 16 as shown in FIG. 3(d). The first metal layer 24 is then patterned and etched such that all of the doped regions 14, 16 have separate contacts as shown in FIG. 4(a)."

(c) "[0038] Returning to the explanation of the fabrication with reference to FIG. 2, after the first metal layer 24 is patterned, processing proceeds to S16 in which the insulator layer 26 made of polyimide (e.g., Hitachi PiX3400 (trade mark) is applied (coated) over the first metal layer 24 to obtain a film thickness of approximately 5 μm, as shown in FIG. 4(b).

[0039] Then, after doing a pre-bake (pre-cure) to eliminate the solvents in the stuck (coated) polyimide, the insulator layer 26 is patterned to pierce the opened windows 44 as shown in FIG. 4(c). More specifically, a thin layer of photoresist (e.g., Shipley 1813 (trade mark)) is formed and the photoresist is exposed to ultraviolet through a photolithography mask (not shown).

[0040] Then, the photoresist is developed using a developer (e.g., Shipley M319 (trademark)). In the development, the polyimide is also etched. Then, a solvent (e.g., n-butyl acetate) is applied to remove the photoresist. In doing this, care should be taken not remove the necessary polyimide portion. Other solvents such as cellosolve acetate could be used for the same purpose.

[0041] In the flow chart of FIG. 2, processing next proceeds to S18 in which the substrate 10 configured as above is heated in a furnace to cure the insulator layer 26 of polyimide. More specifically, the substrate 10 configured as above is baked or heated (in air or nitrogen atmosphere) at 120 degrees C for 30 min., followed by another 30 min. at 200 degrees C, and followed by still another 1 hour at 350 degrees C.

[0042] The process proceeds to S20 in which the substrate 10 configured as above is additionally cured by being baked or heated (in air or in nitrogen atmosphere) at an increased temperature up to 400 degrees C for 30 min. With this additional heating, the insulator layer 26 of polyimide is sufficiently cured and is contracted such that the edges at the opened windows 44 have round and smooth shape. In other words, the insulator layer 26 is relatively planarized and even.

[0043] It should be noted that the temperature and time in the additional curing shown in S20 is an example that depends on the property or kind of the polyimide and the thickness of the insulator layer 26. The inventors have noted that increasing the time up to 1 hour at 400 degrees C was still effective for the purpose, but increasing the temperature to 500 degrees C made the insulator layer 26 too hard and resulted in, cracking at the layer 26.

[0044] The process then proceeds to S22 in which the second metal layer 28 made of a metal stack (at the thickness of 1 to 2 μm) comprising aluminum/chromium/nickel/copper, is deposited on the insulator layer 26 and the first metal layer 24 such that the aluminum layer in the second metal layer 28 and the first metal layer 24 comprising aluminum are joined together by being annealed to form contacts as shown in FIG. 4 (d)."

(d) "[0052] Explaining the method in the second embodiment with reference to FIG. 6, the process begins in S100, after performing processing similar to that of the first embodiment up to S102, processing proceeds to S104 in which the first metal layer 24 of 2 to 4 μm of aluminum is deposited, and then patterning and etching are conducted such that each of the doped regions 14, 16 has an independent setting. Then, processing proceeds to S106 in which the first insulator layer 26a of polyimide (e.g., Hitachi PiX3400 (trade mark)) is applied (coated) over the first metal layer 24 to obtain a film thickness of approximately 2 to 4 μm.

[0053] Then, after doing a pre-bake (pre-cure) to eliminate the solvents in the polyimide, the first insulator layer 26a is patterned to pierce the opened windows 44. More specifically, similar to the first embodiment, a thin film of photoresist (e.g., Shipley 1813 (trade mark)) is formed on the polyimide layer 26 and the photoresist is exposed to ultraviolet through a photolithography mask (not shown).

[0054] Then, the photoresist is developed using a developer (e.g., Shipley M319 (trademark)), while etching the polyimide. The patterning and etching are conducted in such a way that the polyimide film 26a does not encroach on top 240 of the first metal layer 24, as shown in FIG. 7(a). Then, a solvent (e.g., n-butyl acetate)

is applied to remove the photoresist. In doing this, care should be taken not remove the required pattern portion of polyimide. Similar to the first embodiment, other solvents such as cellosolve acetate could be used.

[0055] The process then proceeds to S108 in which the substrate 10 configured as above is heated in a furnace to cure the first insulator layer 26a of polyimide. More specifically, the substrate 10 configured as above is baked or heated (in air or in nitrogen atmosphere) at 120 degrees C for 30 min., followed by another 30 min. at 200 degrees C, and followed by still another 1 hour heated at 350 degrees C.

[0056] It should be noted here that the process in S108 is optional and can be omitted if desired.

[0057] The process then proceeds to S110 in which a second insulator layer 26b of polyimide is applied (coated) over the first insulator layer 26a in a similar fashion. At this time, the second insulator layer 26b is applied (coated) at a much higher speed (that is, in a shorter time) compared with the application (coating) speed of the first insulator layer 26a. The material used in the second insulator layer 26b is the same as that of the first insulator layer 26a, but a less viscous polyimide is used to form much thinner polyimide layer of approximately 1 μm. Next, as shown in FIG. 7(b), the second insulator layer 26b is then patterned and etched in the same way as the first insulator layer 26a to pierce the opened windows 44.

[0058] In this regard, however, the second insulator layer 26b must encroach a little bit on top 240 of the first metal layer 24. In this way, the first insulator layer 26a, 26b are patterned and etched to pierce the opened windows 44 as shown in FIG. 7(c).

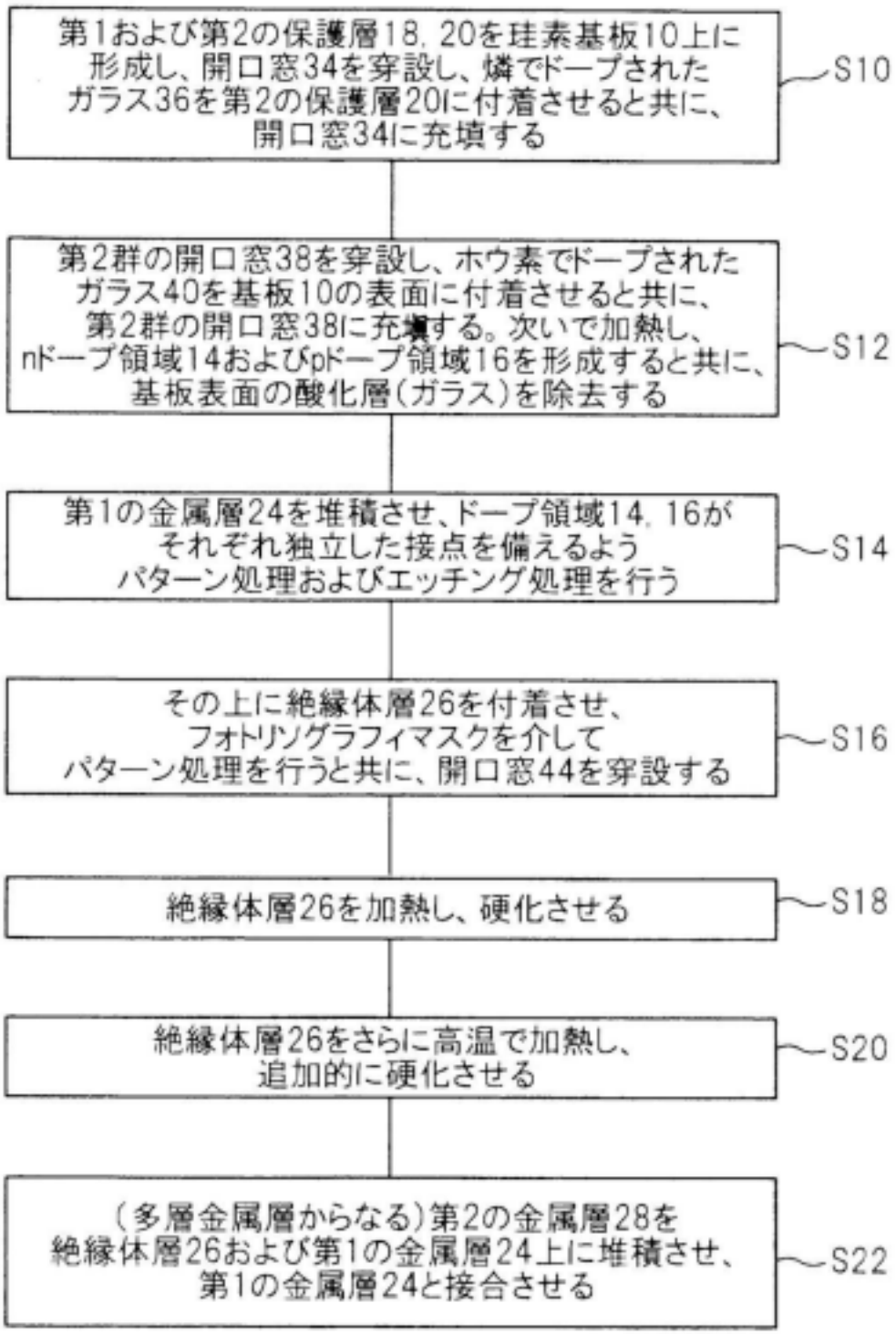
[0059] The process then proceeds to S112 in which the second insulator layer 26b is cured in the same manner as the first insulator layer 26a.

[0060] The process then proceeds to S114 in which the second metal layer 28 made of a metal stack (at the thickness of 1 to 2 μm) similar to that used in the first embodiment is deposited on the second insulator layer 26b and the first metal layer 24 such that the aluminum layer in the second metal layer 28 and aluminum in the first metal layer 24 are joined together by being annealed to form contacts as shown in FIG. 7(d).

[0061] As mentioned above, since the polyimide application (coating) is made twice in the second embodiment, it makes easier to obtain the required of the polyimide layer. As a result, a more planarized insulator layer surface is achieved with less raised edges, and a void is reduced and stress in the electrode substrate 100

is also mitigated, resulting in decreasing the reliability problem of solder fatigue."

(e) "[FIG. 2]



S10 Form the first and second passivating layers 18 and 20 on the silicon substrate

10 by piercing the opened windows 34, and sticking the phosphorus-doped glass 36 to the second passivating layer 20 and filled into the opened windows 34

S12 Pierce the opened windows 38 of the second group, and the boron-doped glass 40 is applied over the surface of the substrate 10 and filled into the opened windows 38 of the second group. Then, apply heat to form the n-doped regions 14 and the p-doped region 16, and remove oxide layers (glasses) on the substrate surface

S14 Deposit the first metal layer 24, and conduct patterning and etching such that doped regions 14, 16 have separate contacts

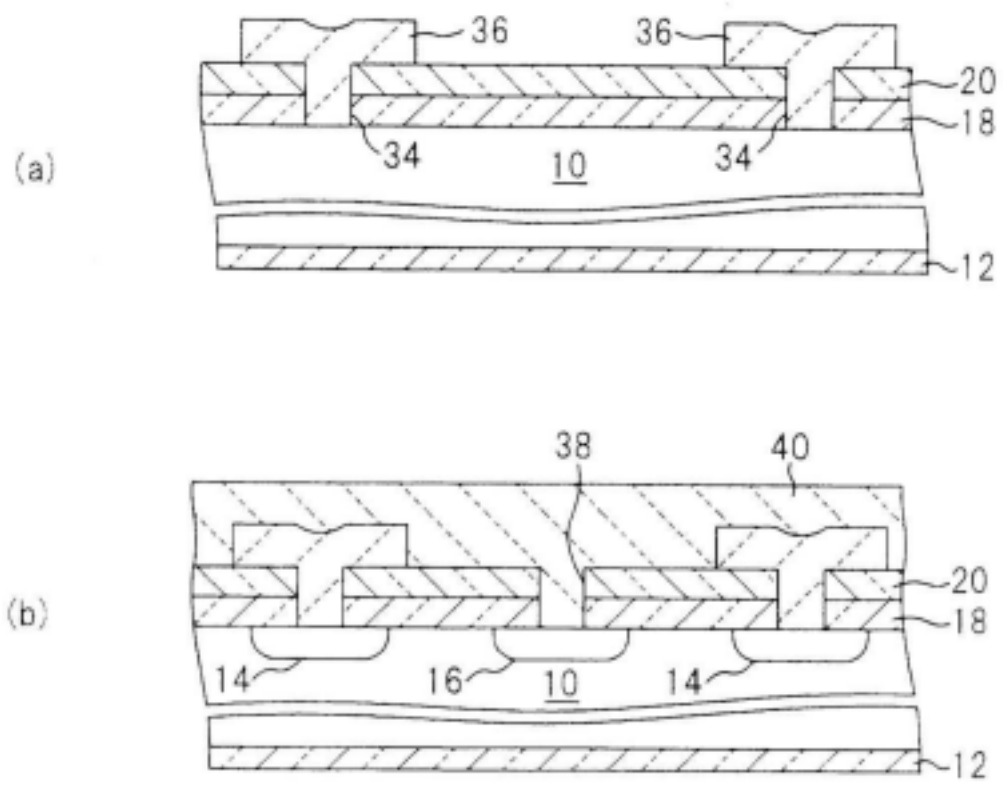
S16 Stick the insulator layer 26 on the first metal layer 24, and conduct patterning through a photolithography mask to pierce the opened windows 44

S18 Heat the insulator layer 26 to make it hardened

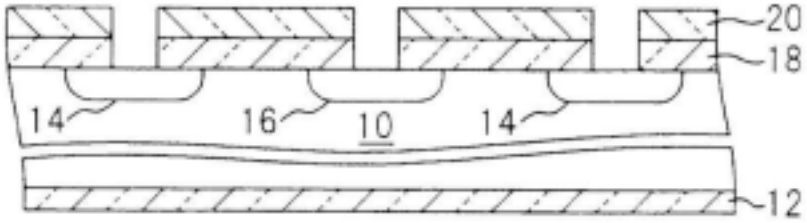
S20 Heat the insulator layer 26 at higher temperature to harden it additionally

S22 Deposit the second metal layer 28 (made of a metal stack) on the insulator layer 26 and the first metal layer 24, and make it be joined with the first metal layer 24

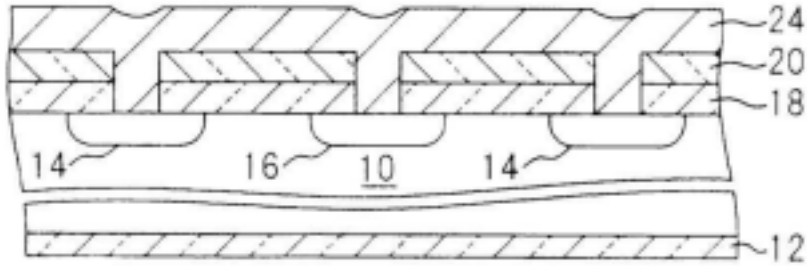
[FIG. 3]



(c)

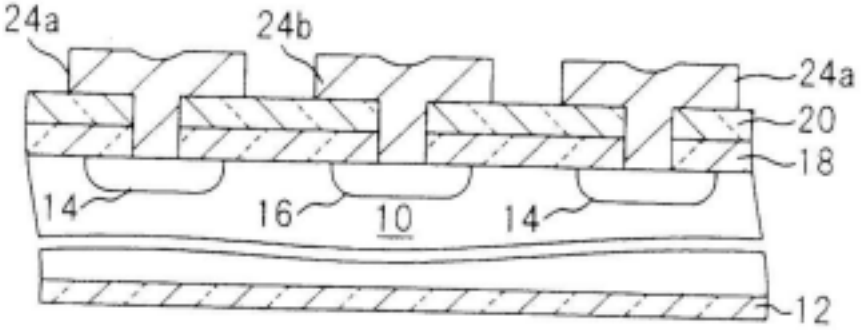

20
18
14
16
10
14
12

(d)

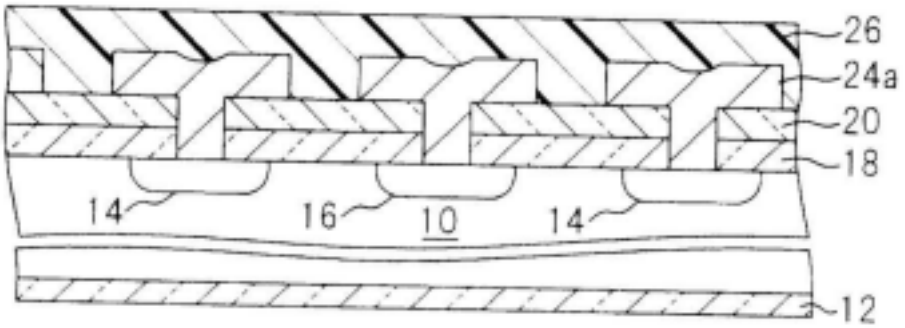

24
20
18
14
16
10
14
12

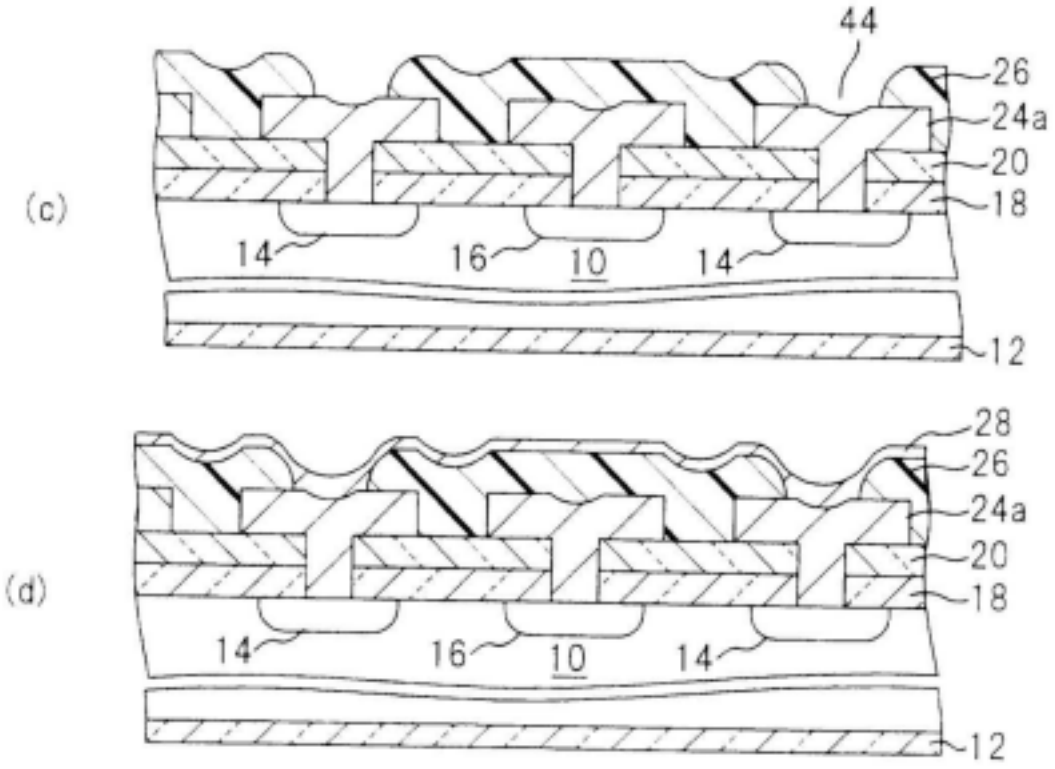
[FIG. 4]

(a)

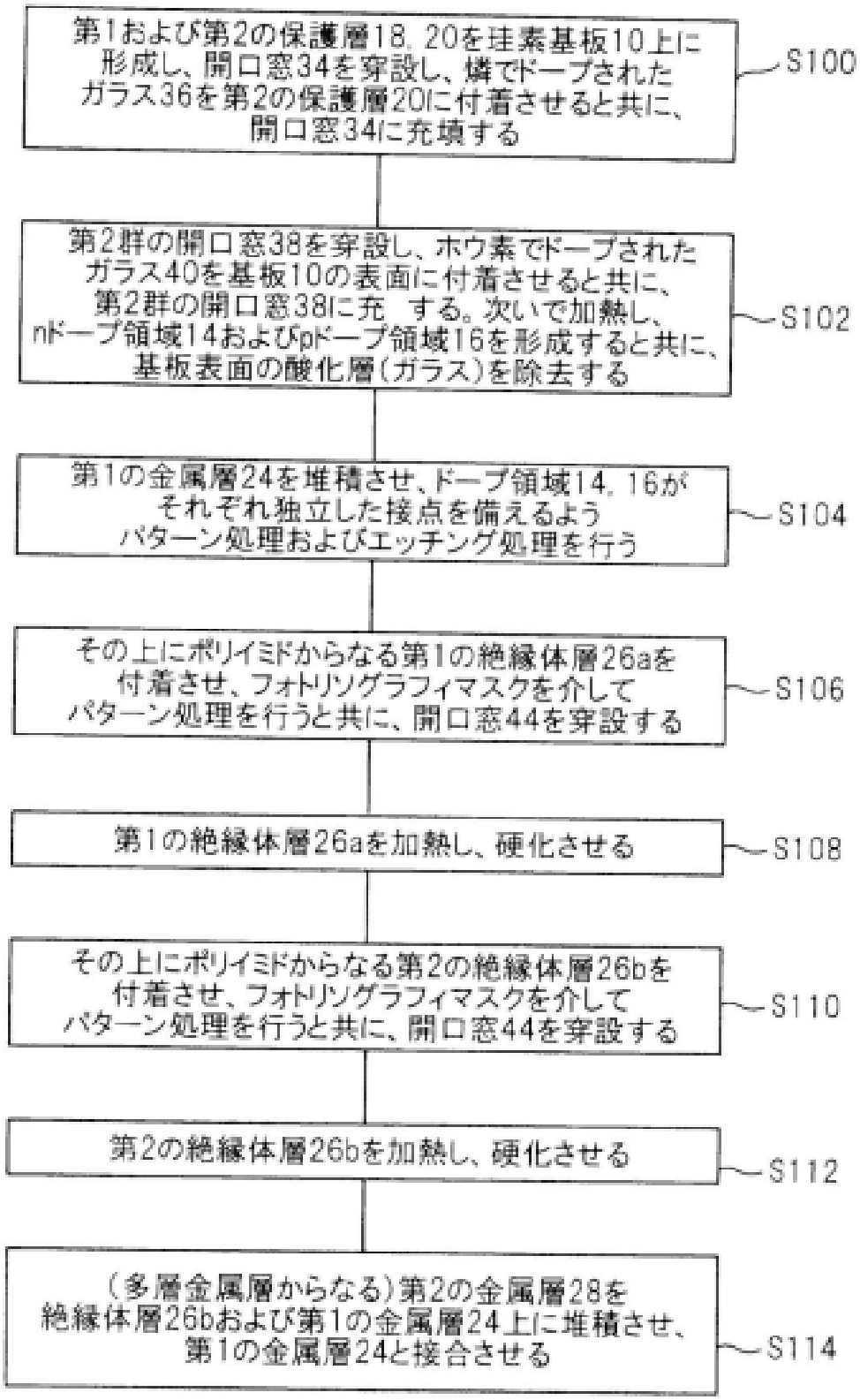

24a
24b
24a
20
18
14
16
10
14
12

(b)


26
24a
20
18
14
16
10
14
12



[FIG. 6]



S100 Form the first and second passivating layers 18 and 20 on the silicon substrate

10 by piercing the opened windows 34, and sticking the phosphorus-doped glass 36 to the second passivating layer 20 and filled into the opened windows 34

S102 Pierce the opened windows 38 of the second group, and the boron-doped glass 40 is applied over the surface of the substrate 10 and filled into the opened windows 38 of the second group. Then, apply heat to form the n-doped regions 14 and p-doped region 16, and remove oxide layers (glasses) on the substrate surface

S104 Deposit the first metal layer 24, and conduct patterning and etching such that doped regions 14, 16 have separate contacts

S106 Stick the insulator layer 26a of polyimide on the substrate, and conduct patterning through a photolithography mask to pierce the opened windows 44

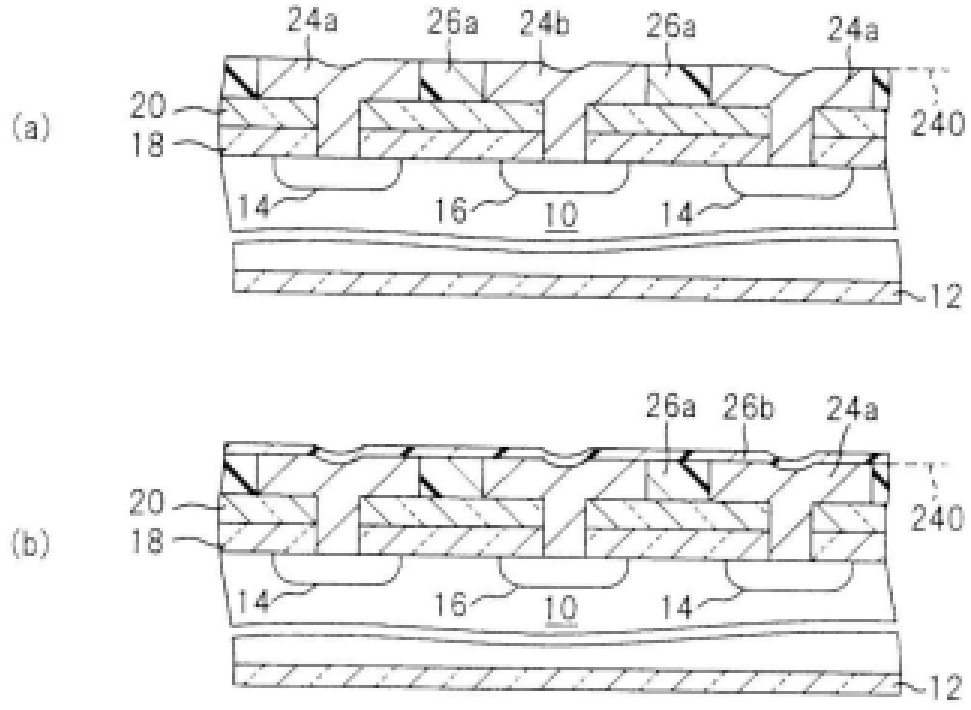
S108 Heat the insulator layer 26a to make it be hardened

S110 Stick the insulator layer 26b made of polyimide on the substrate, and conduct patterning through a photolithography mask to pierce the opened windows 44

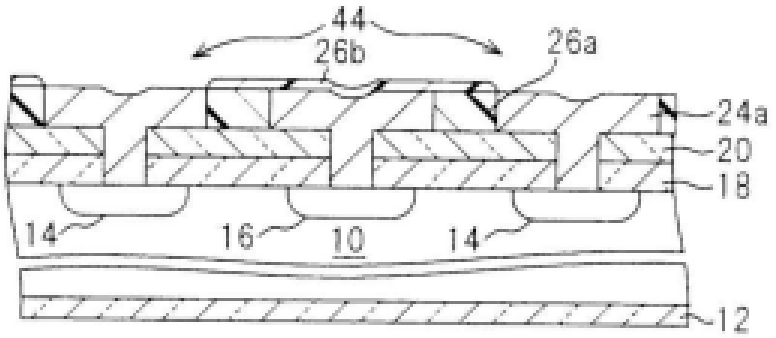
S112 Heat the second insulator layer 26b to make it hardened

S114 Deposit the second metal layer 28 (made of a metal stack) on the insulator layer 26b and the first metal layer 24, and make it be joined with the first metal layer 24

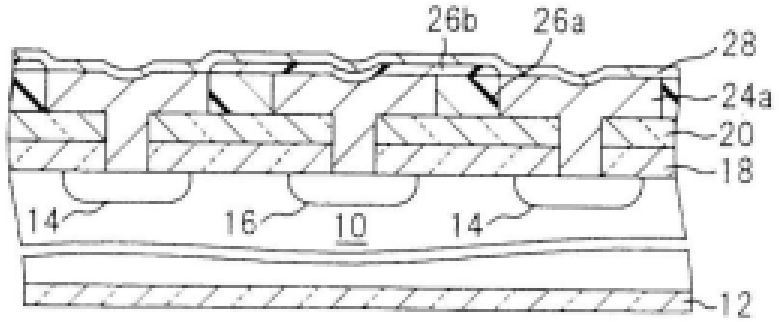
[FIG. 7]



(c)



(d)



"

(f) According to the above-mentioned description (e) relating to [FIG. 4] (c), it is obvious that a plurality of opened windows 44 are pierced in the first insulator layer 26a.

According to the above-mentioned description of Cited Document 1, it discloses the following invention (hereinafter, referred to as "Cited Invention").

"A method of fabricating a solar cell, the method comprising:

forming a first passivating layer 18 made of oxidized silicon on a substrate 10, forming a second passivating layer 20 made of silicon nitride over the first passivating layer 18, piercing the opened windows 34 in the first and second passivating layers 18 and 20 to expose the surface of the substrate 10, and sticking the phosphorus-doped glass 36 to the second passivating layer 20 to fill the opened windows 34;

between the first-pierced opened windows 34 of the first group, piercing the opened windows 38 of the second group, respectively; sticking the boron-doped glass 40 to the surface of the substrate 10 to fill the opened windows 38 of the second group; making dopants in the doped glasses 36, 40 to be diffused into a surface of the substrate 10 to form an n-doped region 14 and a p-doped region 16;

removing all of the glasses 36, 40 on the substrate surface;
after the first metal layer 24 is deposited,
conducting patterning and etching such that all of the doped regions 14, 16 have separate setting,
and sticking a first insulator layer 26a made of polyimide on the first metal layer 24;
patterning is conducted to the first insulator layer 26a to pierce an opened windows 44,
and, more specifically, a thin film of photoresist is formed on the polyimide layer 26, making the photoresist film be exposed to ultraviolet light through a photolithography mask, developing the photoresist film using a developer, and etching the polyimide to pierce a plurality of the opened windows 44"

(2) Cited Document 2

Japanese Unexamined Patent Application Publication No. 2002-158248 (hereinafter, referred to as "Cited Document 2"), which was cited in the Reason for Refusal, the Decision of Refusal, and the Reconsideration Report, and had been distributed in advance of the priority date of the present application shows the following matters. (The underlines are added by the body.)

(a) "[0057] An insulating film 14 is formed on a face provided with the pad 12 of the semiconductor chip 10. The insulating film 14 is formed so as to cover each pad 12. In this embodiment, the insulating film 14 is formed of a single layer, but may be formed of a plurality of layers, as shown in an example described below. The thickness of the insulating film 14 can be determined depending on the requirement. The insulating film 14 may be a general passivation film. The insulating film 14 can be formed of, for example, SiO_2, SiN, or a polyimide resin. In this embodiment, a step for exposing at least a part of each pad 12 from the insulating film 14 and a step for forming a bump on the pad 12 can be performed using the same resist layer 20. In detail, these steps can be performed using the same resist layer 20 that has been formed, without forming resist layer 20 repeatedly.
[0058] As shown in FIG. 2(A), the resist layer 20 is formed. The resist layer 20 is formed on the face provided with the pads 12 of the semiconductor chip 10; that is, on the insulating film 14. The resist layer 20 has through holes 22 above the pads 12. The through holes 22 may be formed by a photolithographic technique. That is, a photosensitive resist layer 20 is irradiated with energy and is developed to form the through holes 22 through a mask. In this case, the resist layer 20 may be of a positive type or a negative type. The resist layer 20 may have a thickness of

approximately 20 μm.

[0059] The through holes 22 may be formed by etching a non-photosensitive resist layer 20. Alternatively, the resist layer 20 may be formed by a screen printing process or an inkjet process.

[0060] The through hole 22 are preferably formed so as to have a shape which does not protrude from the peripheries of the pads 12. A bump can thereby be formed on each of the plurality of pads 12 provided at a narrow pitch. The through holes 22 are preferably formed so as to have walls perpendicular to the face of the semiconductor chip 10. Bumps which vertically extend can thereby be formed. The planar shape of the through holes 22 is not limited and may be, for example, circular or rectangular.

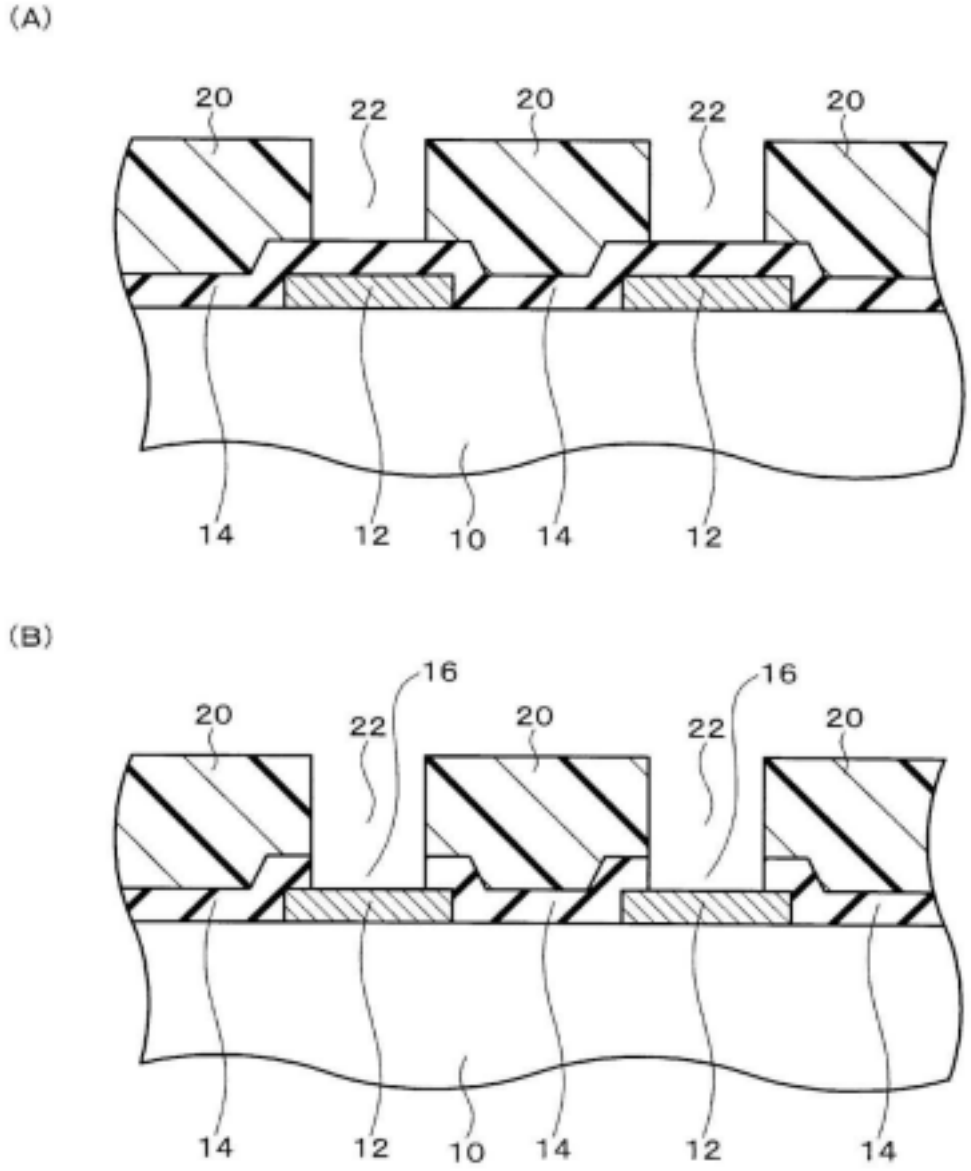
[0061] As shown in FIG. 2(B), the portions of the insulating film 14 in the through holes 22 are removed through the resist layer 20 as mask to form openings 16 so that at least parts of pads 12 are exposed. The openings 16 can be formed by etching. The etching process may be any one of a chemical process, physical process, and a combination thereof. The etching characteristics may be isotropic or anisotropic. As described below, isotropic etching which etches equally in all directions can be applied to the present invention."

(b) "[0083] In this embodiment, as shown in FIG. 7(A), a semiconductor chip 10 provided with an insulating layer 15 is prepared. The insulating layer 15 is thinner at a portion which covers the center of each pad 12 than at a portion which covers the surface of the semiconductor chip 10 and the end of the pad 12. The insulating layer 15 may be formed of a single layer or a plurality of layers. For example, as shown in FIG. 7(A), the insulating layer 15 may be formed of an upper layer 50 and a lower layer 60. In this case, the lower layer 60 has openings 62 in the central portions of the pads 12 and covers the surface of the semiconductor chip 10 and the ends of the pads 12. The upper layer 50 is formed on the lower layer 60 and the central portion of each pad 12. In such a manner, a thin portion 17 of the insulating layer 15 may be formed in the central portion of each pad 12.

[0084] As shown in FIG. 7(A), a resist layer 20 having through holes 22 is formed on the insulating layer 15 of the semiconductor chip 10. Each through hole 22 may be formed at the inner side of the periphery of the pad 12 and at the outer side of the thin portion 17 of the insulating layer 15. When the insulating layer 15 is formed of the upper layer 50 and the lower layer 60, the wall of each through hole 22 may be formed above a portion, which covers the end of the corresponding pad 12, of the lower layer 60. When the portion of the insulating layer 15 in the through hole

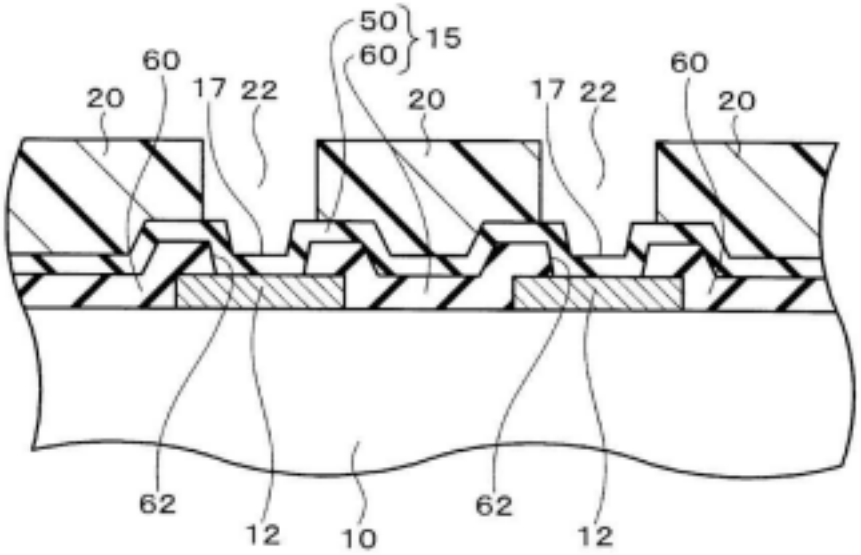
22 is removed, the opening is readily formed in the insulating layer 15 so as not be larger than the through hole 22. In detail, etching is performed with a time and processing performance of a degree for removing at least a part of the thin portion 17 of the insulating layer 15 without removing the thick portions of the insulating layer 15. As a result, the opening is formed in the insulating layer 15 so as not larger than the through hole 22."

(c) "[FIG. 2]

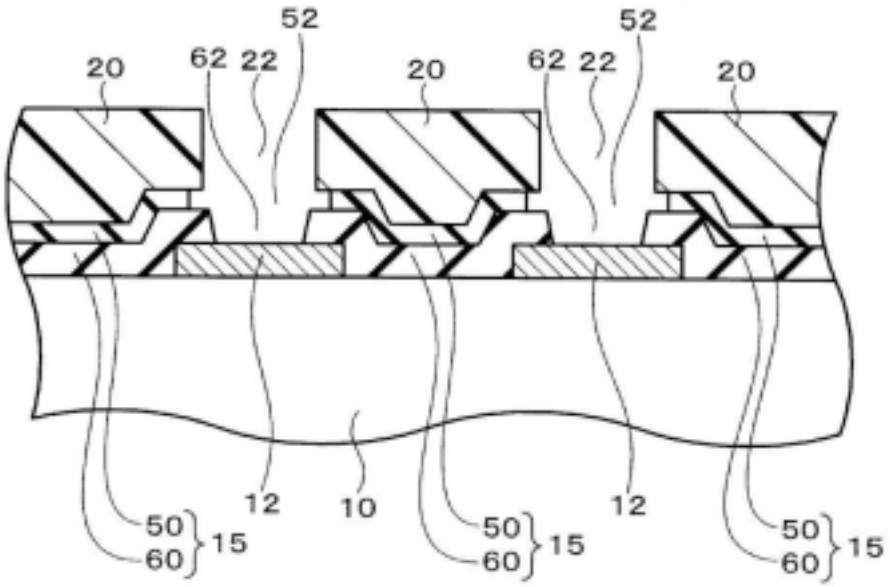


[FIG. 7]

(A)



(B)



"

Consequently, Cited Document 2 discloses as follows.

"technical matters that: the semiconductor chip 10 provided with an insulating layer 15 is prepared; the insulating layer 15 is formed of an upper layer 50 and a lower

layer 60; the lower layer 60 has openings 62 in the central portions of the pads 12 and covers the surface of the semiconductor chip 10 and the ends of the pads 12; the upper layer 50 is formed on the lower layer 60 and the central portion of each pad 12; a resist layer 20 having through holes 22 is formed on the insulating layer 15; the insulating film 14 can be formed of for example, SiO_2, SiN, or a polyimide resin; and the resist layer 20 may be formed by a screen printing process or an inkjet method" (hereinafter, referred to as "the technical matters of the Cited Document 2").

(3) Cited Document 3

Japanese Unexamined Patent Application Publication No. 2006-124805 (hereinafter, referred to as "Cited Document 3"), which was cited in the Reconsideration Report and had been distributed in advance of the priority date of the present application, shows the following matters. (The underlines are added by the body.)

(a) "[0026]

Hereinafter, based on the embodiments indicated in the drawings, the present invention will be described in detail.

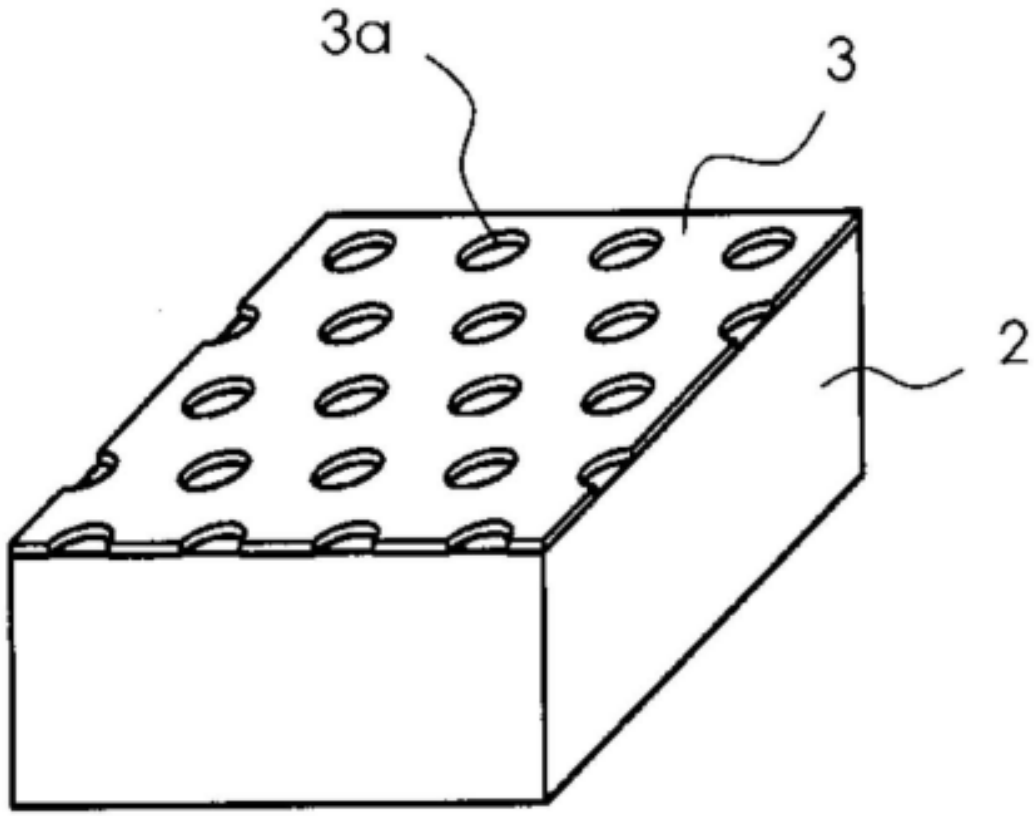
First, a method of fabricating foil according to a first embodiment of the present invention will be described referring to the fragmentary perspective view shown in FIG. 1 schematically.

As shown in the figure, a mesh-patterned mask pattern 3 is printed to a foil 2 by a printing machine using an inkjet method. In the mesh-patterned mask pattern, a round-shaped hole portion is an opening 3a to which ink is not printed.

Here, it is preferred that the ink be made from materials not etched by chemicals used for etching of the foil 2 which are discussed below, and there may be used ink or inorganic sol dispersion liquid including any of or some of resin, half polymer, monomer that become hardened by heat or ultraviolet light.

Meanwhile, in the present invention, although the mask includes a mask pattern 3 to which ink has been printed and the opening 3a to which ink has not been printed, the portion to which the ink has been printed is called the mask pattern 3 accordingly."

(b) "[FIG. 1]



"

Consequently, Cited Document 3 discloses "technical matters that: to the foil 2, the mesh-patterned mask pattern 3 is printed by a printing machine using an inkjet method; and, in the mesh-patterned mask pattern, a round-shaped hole portion is the opening 3a to which ink has not been printed" (hereinafter, referred to as "the technical matters of Cited Document 3").

(4) Cited Document 4

Japanese Unexamined Patent Application Publication No. 2004-209887 (hereinafter, referred to as "Cited Document 4"), which was cited in the Reconsideration Report and is a publication and had been distributed in advance of the priority date of the present application shows the following matters. (The underlines are added by the body.)

(a) "[0001]

[Technical Field]

The present invention relates to a liquid ejection apparatus to eject liquid on a medium. In addition, it relates to liquid ejection method, a program, and a computer

system using such liquid ejection apparatus.

[0002]

[Background Art]

As a printer to print an image on various kinds of media such as a paper, a fabric, and a film, there is known an inkjet printer to perform printing by ejecting ink. In such an inkjet printer, printing is performed by repeating a printing operation (ejection operation) to eject ink from a nozzle, and a transportation operation (moving operation) to move mediums in a transportation direction one after the other."

(b) "[0021]

<Banding >

FIG. 13A is a description diagram of a dot line (also referred to as a raster line) formed on a printing sheet. In this diagram, a dot line is formed on a printing sheet that is a medium such as a paper by a band printing method. The 'band printing method' is a printing method to form continuing dot lines by a single pass. The 'pass' means an operation in which a head moves in the scanning direction and ejects ink intermittently while moving."

(c) "[0116]

FIG. 24 is a description diagram of a dot line formed on a printing sheet P. As compared with the case of FIG. 13A, it is identical in a point that dots are formed in 80% of pixels, but the diameter of a dot formed on a printing sheet is small. As can be seen by comparing FIG. 24 and FIG. 13A, if an ejected ink drop is small (if a dot formed on the printing sheet P is small), an amount of ink that intermingles between dot lines will be small. In addition, if an ejected ink drop is large (if a dot formed on the printing sheet P is large), an amount of ink that intermingles between dot lines will be large. In this way, a state of intermingling of ink differs according to the size of an ink drop ejected from a nozzle."

(d) "[0130]

FIG. 26 is a description diagram of a dot line formed by a pseudo band printing method. The 'pseudo band printing method' is a printing method in which continuing dot lines are completed by multiple passes (printing operations). In the present embodiment, continuing dot lines are completed by two passes. Because the interval between nozzles is 180 dpi, an interval D of dot lines formed on a printing sheet will be 360 dpi."

(e) "[FIG. 13] (80%)

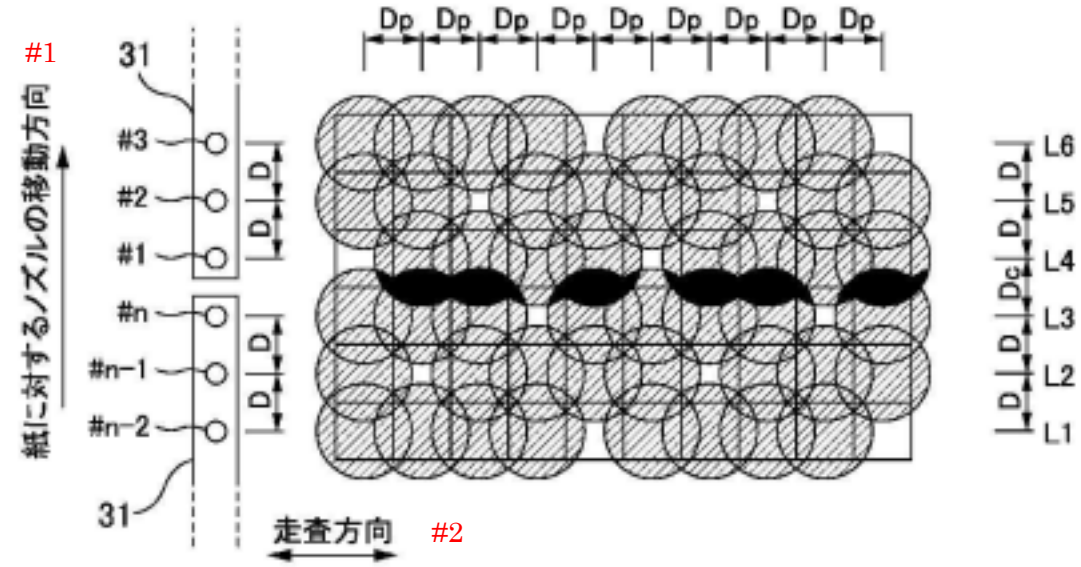


図13A(80%) #3

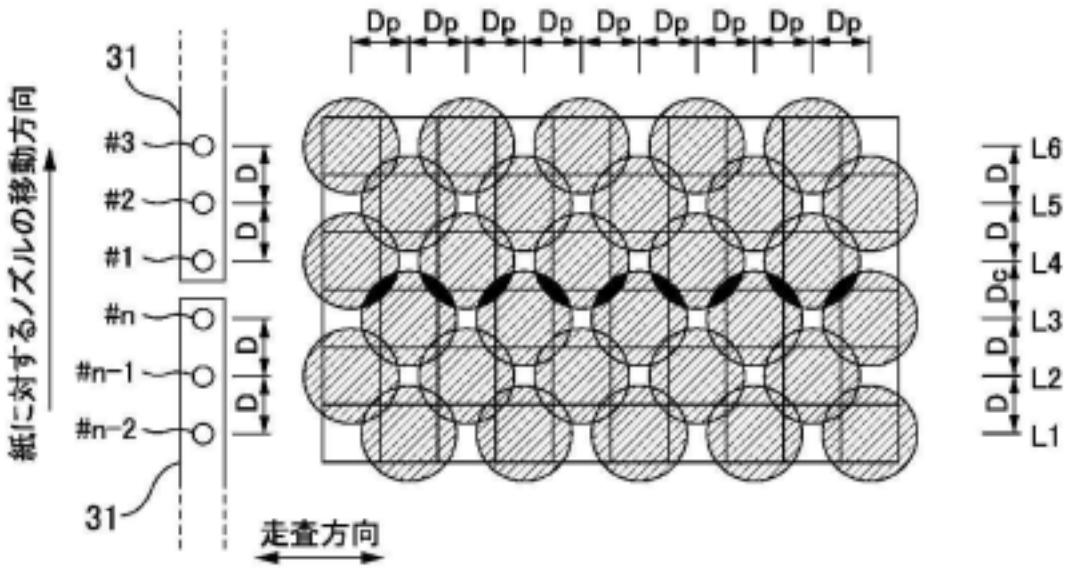


図13B(50%) #4

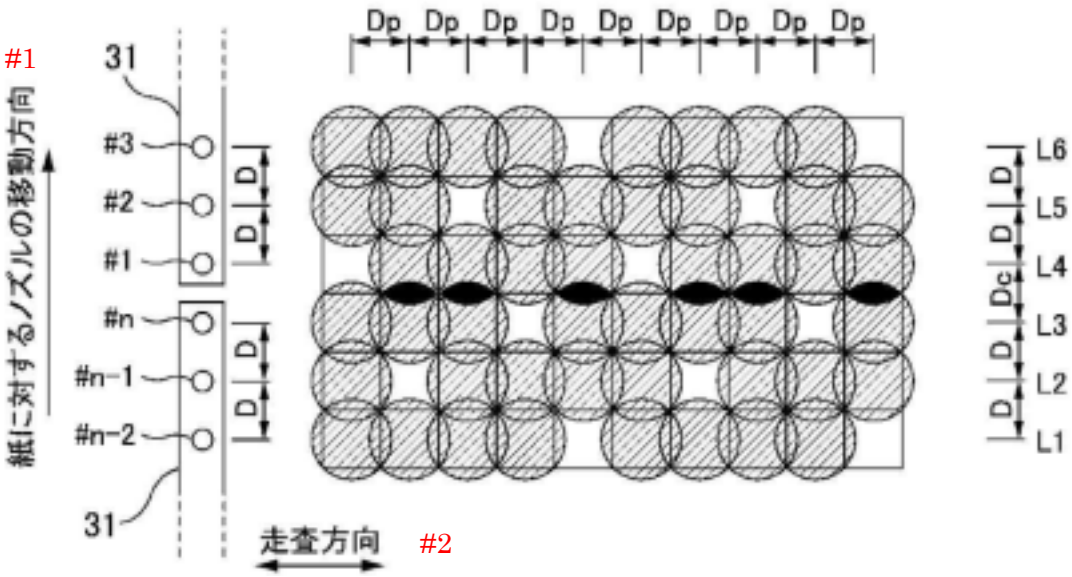
#1 Moving direction of nozzles relative to paper

#2 Scanning direction

#3 FIG. 13A (80%)

#4 FIG. 13B (50%)

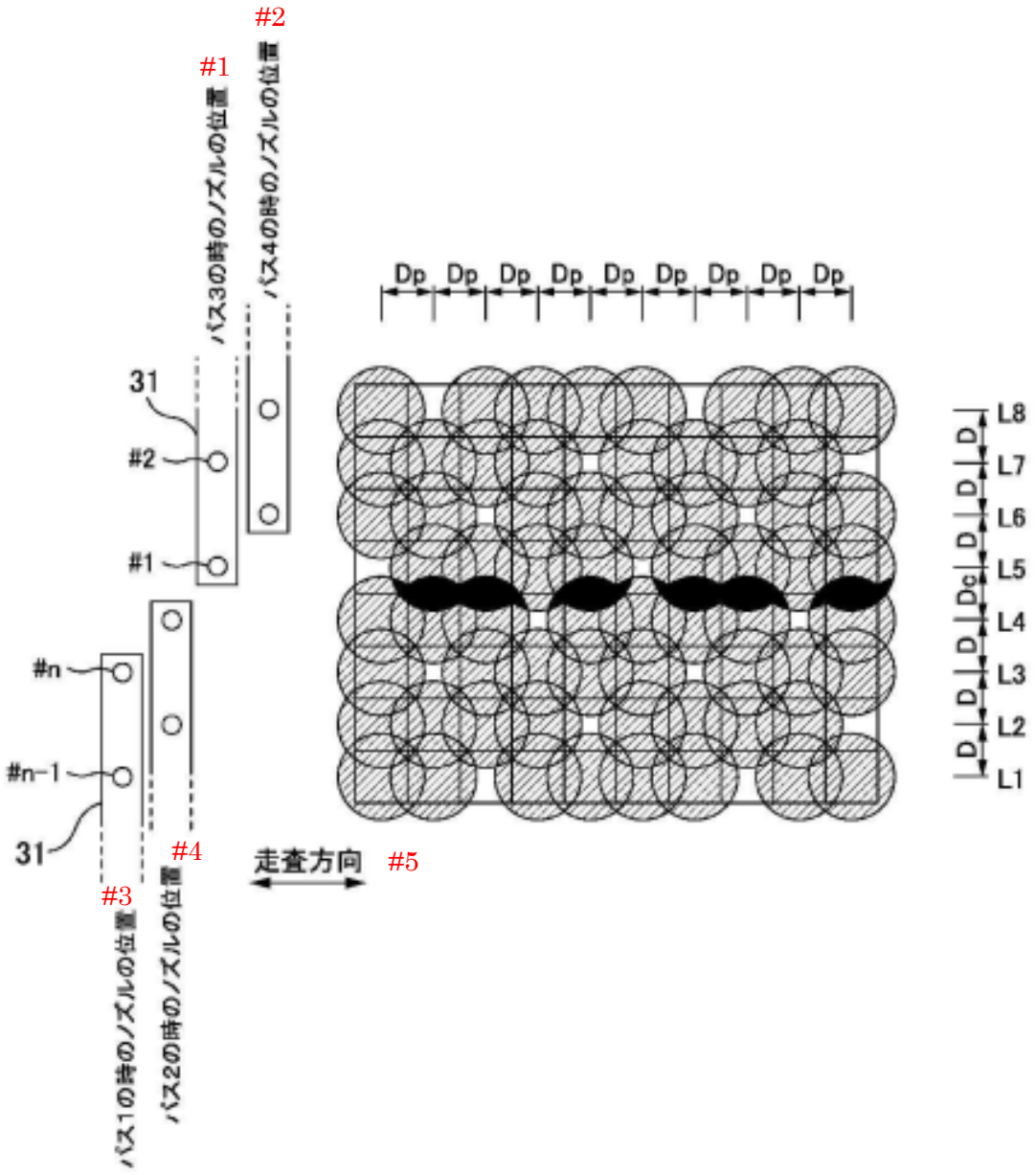
[FIG. 24]



#1 Moving direction of nozzles relative to paper

#2 Scanning direction

[FIG. 26]



#1 Nozzle position at pass 3

#2 Nozzle position at pass 4

#3 Nozzle position at pass 1

#4 Nozzle position at pass 2

#5 Scanning direction

"

(f) According to the descriptions of the above-mentioned (b) to (d), in FIG. 13, FIG. 24, and FIG. 26 of (e), dot lines formed by a liquid ejection apparatus are graphically illustrated and there exist openings where ink has not been ejected and dots are not formed in the dot lines.

Consequently, the above-mentioned Cited Document 4 discloses "technical matters that, in dot lines formed by a liquid ejection apparatus, there exist openings in the dot lines, a dot not being formed in the openings, in areas where ink has not been ejected" (hereinafter, referred to as "the technical matters of Cited Document 4").

(5) Comparison

The Amended Invention 1 is compared with the Cited Invention.

(a) "The substrate 10," "the first insulator layer 26a," and "the method of fabricating a solar cell" of the Cited Invention correspond to "wafer," "the second dielectric layer," and "the method of fabricating solar cell" of the Amended Invention 1, respectively.

(b) Regarding "the substrate 10" of the Cited Invention, it is obvious that, by "forming the n-doped region 14 and the p-doped region 16 by performing diffusion into the surface of the substrate 10," it is processed into one component of a solar cell, and, thus, "the substrate 10" onto which "the n-doped region 14 and the p-doped region 16 are formed by performing diffusion into its surface" corresponds to "a wafer to be processed into a solar cell" of the Amended Invention 1.

(c) Since both "the first passivating layer 18 made of oxidized silicon" and "the second passivating layer 20 made of silicon nitride" of the Cited Invention are films formed of dielectric, "the first and second passivating layers 18 and 20" of the Cited Invention correspond to "the first dielectric layer" of the Amended Invention 1.

In addition, the structure of "the first passivating layer 18 of oxidized silicon is formed on the substrate 10, and the second passivating layer 20 made of silicon nitride is formed on the top surface of the first passivating layer 18" of the Cited Invention corresponds to the structure of "forming the first dielectric layer over a wafer" of the Amended Invention 1.

(d) "The first insulator layer 26a" of the Cited Invention is one that is formed by "piercing the opened windows 34 into the first and second passivating layers 18 and 20 to expose the surface of the substrate 10; sticking the phosphorus-doped glass 36 to the second passivating layer 20, and filling the glass 36 into the opened windows 34; between the first-pierced opened windows 34 of the first group, piercing the

opened windows 38 of the second group, respectively; sticking the boron-doped glass 40 to the surface of the substrate 10, and filling the glass 40 into the opened windows 38 of the second group; making dopants in the doped glasses 36 and 40 to be diffused into the surface of the substrate 10 to form the n-doped region 14 and the p-doped region 16; removing all of the glasses 36 and 40 on the substrate surface; after the first metal layer 24 is deposed, conducting patterning and etching such that all of the doped regions 14 and 16 have separate setting; sticking the first insulator layer 26a made of polyimide to the first metal layer 24; and conducting patterning and etching to the first insulator layer 26a to pierce a plurality of opened windows 44". Therefore, it is obvious that a plurality of the first insulator layer 26a are formed over "the first and second passivating layers 18 and 20" between patterns of the first metal layer 24 for which patterning has been conducted. Consequently, the structure to form "the first insulator layer 26a" by "piercing the opened windows 34 into the first and second passivating layers 18 and 20 to expose the surface of the substrate 10; sticking the phosphorus-doped glass 36 to the second passivating layer 20, and filling the glass 36 into the opened windows 34; between the first-pierced opened windows 34 of the first group, piercing the opened windows 38 of the second group, respectively; sticking the boron-doped glass 40 to the surface of the substrate 10, and filling the glass 40 into the opened windows 38 of the second group; making dopants of the doped glasses 36 and 40 to be diffused into the surface of the substrate 10 to form the n-doped region 14 and the p-doped region 16; removing all the glasses 36 and 40 on the substrate surface; after depositing the first metal layer 24, conducting patterning and etching such that all of the doped regions 14 and 16 have separate setting; sticking the first insulator layer 26a made of polyimide to the first metal layer 24; and conducting patterning to the first insulator layer 26a to pierce a plurality of the opened windows 44" corresponds to the structure to "form a plurality of second dielectric layers over the first dielectric layer" of the Amended Invention 1.

In addition, "a plurality of opened windows 44" of the above-mentioned Cited Invention that are "pierced" into " the first insulator layer 26a" that have been formed plurally correspond to "a plurality of openings" "between a plurality of second dielectric layers" of the Amended Invention 1.

(e) In the Cited Invention, it is obvious that a "photoresist film" is formed after forming " the first insulator layer 26a," and it is also obvious that the "photoresist film" has an opening for "piercing the opened windows 44" into " the first insulator layer 26a."

In addition, it is obvious that "a plurality of dots" of the Amended Invention 1 is formed after forming a "second dielectric layer."

Therefore, the structure of the Cited Invention of "patterning to the first insulator layer 26a, is conducted to pierce the opened windows 44, and, more specifically, a thin film of photoresist is formed on the polyimide layer 26, making the photoresist film be exposed to ultraviolet light through a photolithography mask, developing the photoresist film using a developer, and etching the polyimide to pierce a plurality of the opened windows 44," and the structure of the Amended Invention 1 of "inkjet printing a plurality of dots at least in a plurality of openings between the plurality of second dielectric layers to form a plurality of gaps formed by intersections of the plurality of dots and having a smaller area than an area of the plurality of dots, wherein the size of the gap is determined by at least (i) an alignment of a plurality of inkjet printer nozzles that supply the plurality of dots, (ii) the size of the plurality of dots, and (iii) which nozzles are used" are common in "forming a film having a plurality of gaps after forming the second dielectric layer."

(6) Identical feature

Consequently, the Amended Invention 1 and Cited Invention are identical in the viewpoint of

"a method of fabricating a solar cell that: includes

forming a first dielectric layer over a wafer to be processed into a solar cell; and

forming a plurality of second dielectric layers over the first dielectric layer;

includes forming a film having a plurality of gaps after forming the second dielectric layers; and

providing a plurality of openings between the plurality of second dielectric layers,"

However, there exists differences between them in the following the different feature.

(7) The different feature

A. In the Amended Invention 1, "a plurality of dots are printed by inkjet printing," "a plurality of gaps formed by intersections of the dots and having a smaller area than an area of the plurality of dots are formed, a size of the gaps being dictated at least by (i) an alignment of a plurality of inkjet printer nozzles that supply the plurality of dots, (ii) the size of the plurality of dots, and (iii) which nozzles are used,"

and "the plurality of dots" are printed over "at least a plurality of openings between the plurality of second dielectric layers," whereas, in the Cited Invention, a film-forming method of a "photoresist film" is undefined, and how an opening for "piercing the opened windows 44" of the "photoresist film" is formed is undefined and its size is also undefined, and, there is no statement of "a plurality of dots" in the Cited Invention, and, therefore, whether or not "a plurality of dots" are formed in "at least a plurality of openings between the plurality of second dielectric layers" is not undefined.

(8) Judgment

As shown in the Cited Document 2 and the Cited Document 3, it is well-known to form a resist mask pattern by means of the inkjet printing method, and there are no factors that prevent the employment of the above-mentioned well-known technique to the Cited Invention.

Therefore, it could be easily derived by a person skilled in the art to form "the photoresist film" over "the first insulator layer 26a" by "inkjet printing a plurality of dots" by means of applying the well-known resist mask pattern forming technique in inkjet printing method to the technique of forming a "photoresist film" in the Cited Invention.

However, in the above-mentioned well-known inkjet method, it is normal to form a pattern by making a plurality of dots in a row and arbitrary-shaped openings in areas where dots are not formed. In that sense, it can be said that the size of the opening is determined by an arrangement of inkjet printer nozzles, the size of a dot, and nozzles selectively used. Yet, the above-mentioned well-known inkjet method to form a pattern by making a plurality of dots in a row and obtain arbitrary-shaped openings in areas where dots are not formed is not one that "to form a plurality of gaps formed by intersections of the dots and having a smaller area than an area of the plurality of dots" as disclosed in the Amended Invention 1.

In addition, while the technical matter of the Cited Document 4 is a well-known technique in a liquid ejection apparatus in which, in dot lines formed by a liquid ejection apparatus, there exist openings in the dot lines, a dot not being formed in the openings, in areas where ink has not been ejected, it is a technical matter that, as described as Background Art in [0002] of the Cited Document 4, relates to "an inkjet printer that performs printing by ejecting ink as a printer to print an image on various kinds of media such as a paper, fabric, film and the like". Therefore, the

well-known art in question is not one that provides an area in which dots are not formed so as to form an opening, but one in which " there exist openings in the dot lines, a dot not being formed in the openings, in areas where ink has not been ejected" as a result of drawing an image of a printing target by dots of ink.

On the other hand, a "gap" in the structure "inkjet printing a plurality of dots to form a plurality of gaps formed by intersections of the plurality of dots and having a smaller area than an area of the plurality of dots" of the Amended Invention 1 corresponds to an opening of a contact mask used as an etching mask, as described in [0017] to [0020] of the description of the present application as

"[0017]

In FIG. 4, a top view showing a positional relationship between a gap 321 and pieces of adjacent dot 306 according to an aspect of the present invention is shown. In the example of FIG. 4, the contact mask 400 includes a plurality of overlapping pieces of dot 306 that have been printed by inkjet printing so as to form the gap 321. The gap 321 is an area where the dot 306 has not been printed. As shown in FIG. 4, each gap 321 may be formed by intersections of a plurality of (for example, four) overlapped pieces of dot 306. Advantageously, the size and position of the gap 321 can be prescribed and decided by a physical alignment of nozzles that supply the dot 306. For example, a dimension 401 between the centers of pieces of dot 306 can be prescribed by a pitch of inkjet nozzles. Therefore, an interval between gaps is determined also by a physical alignment of nozzles supplying dots. ... (Omitted) ...

[0020]

Then, in FIG. 3C, in order to remove a portion of the layer 304 to form a contact area 311 that extends entirely through the layer 304, the contact mask 400 is utilized. In one aspect, the contact area 311 is formed by etching the layer 304 using the contact mask 400 as an etching mask and, in addition, using etchant that does not etch the layer 305 significantly. For example, in the case of the layer 304 including silicon dioxide and the layer 305 including polyimide, the contact area 311 can be formed by applying wet etching, in a buffered oxide etch (BOE) process that uses hydrofluoric acid as etchant, to the exposed portion of the layer 304 (that is, the portion under the gap 321). The layer 305 works as an etch stop layer in such an etching process. FIG. 3C shows the sample of FIG. 3B after the BOE process and the following process of removing the contact mask 400. The contact mask 400 including hot-melt resin can be removed by a mask strip process that uses potassium hydroxide (KOH)". Therefore, this structure is a structure "to form a plurality of gaps formed by intersections of the plurality of dots and having a smaller area than an

area of the plurality of dots" as an opening capable of being used as an etching mask.

For that reason, even if it is trivial, from the technical matter of the Cited Document 4, to obtain dot lines having openings where dots are not formed by not ejecting ink by a liquid ejection apparatus, the relevant technical matter of the Cited Document 4 is one in which "there exist openings in the dot lines, a dot not being formed in the openings, in areas where ink has not been ejected" as a result of drawing an image of a printing target by dots of ink, but not one to form dots in a manner "to form a plurality of gaps formed by intersections of the plurality of dots, the plurality of gaps having a smaller area than an area of the plurality of dots." Therefore, it cannot be said that it is also trivial "to form a plurality of gaps formed by intersections of the plurality of dots, the plurality of gaps having an area smaller than an area of the plurality of dots" as an opening that can be used as an etching mask as is the case with the Amended Invention 1, based on the technical matters of Cited Document 4.

In addition, Cited Document 1 to 3 don’t disclose a plurality of gaps being formed by intersections of the plurality of dots and having a smaller area than an area of the plurality of dots as a part of openings that can be used as etching mask.

Furthermore, even if, by applying the resist mask pattern forming technique according to the well-known inkjet method to the technique for forming a "photoresist film" of the Cited Invention as mentioned above, a structure to form a "photoresist film" on "the first insulator layer 26a" by "inkjet printing a plurality of dots" is made, there is no statements in any of the Cited Invention and Cited Documents 2 to 4 about the structure of "inkjet printing a plurality of dots on at least a plurality of openings between the plurality of second dielectric layers" of the Amended Invention 1, and the structure in question is not common general knowledge.

Therefore, the structure of "inkjet printing a plurality of dots in at least a plurality of openings between the plurality of second dielectric layers" of the Amended Invention 1 could not have been easily derived based on the well-known art described in the Cited Invention, Cited Documents 2 to 3, and Cited Document 4.

Accordingly, even based on the well-known art described in the Cited Invention and Cited Document 2 to 3, and the well-known art described in Cited Document 4, the structure relating to the above-mentioned different feature 1 cannot be obtained.

(9) Conclusion

Since it cannot be said that the Amended Invention 1 could have been easily invented by a person skilled in the art on the basis of the well-known art disclosed in the Cited Invention and Cited Documents 2 to 3, and the well-known art disclosed in Cited Document 4, the Amended Invention 1 complies with the provisions of Article 29(2) of the Patent Act.

In addition, beyond that, there is no other reason that denies the patentability.

2. About the Amended Inventions 2 to 7

Since all of the Amended Inventions 2 to 7 contain the subject matter of the Amended Invention 1, likewise, they could not been easily invented by a person skilled in the art on the basis of the technical matters disclosed in the Cited Invention and the Cited Documents 2 to 4.

Consequently, it can be denied that the Amended Inventions 2 to 7 cannot obtain a patent in accordance with the provisions of Article 29(2) of the Patent Act.

In addition, beyond that, there is no other reason to deny their patentability.

3. About the Amended Invention 8

(1) Cited Documents 1 to 4

The statement contents of the Cited Documents 1 to 4, the described matters of the Cited Invention, and the Cited Documents 2 to 4 are as described in the above-mentioned "1. About the Amended Invention 1" (1) to (4).

(2) Cited Document 5

Japanese Unexamined Patent Application Publication No. 2006-261089 (hereinafter, referred to as "Cited Document 5"), which was cited in the Reason for Refusal, the Decision of Refusal and the Reconsideration Report, and had been distributed in advance of the priority date of the present application, shows the following matters. (The underlines are added by the body.)

(a) "[0001]
The present invention relates to a dye-sensitized solar cell element."

(b) "[0064]
(Example 1)

In order to screen print titania paste on a SnO_2:F glass of a surface resistance value of 12 Ω/sq and of 20 cm square (one that is a transparent conducting glass in

which a SnO_2:F film is formed on a glass substrate, the transparent conducting glass having an opening of 1 mmφ at a distance of about 15 mm from a side of the glass), titania paste Ti-Nanoxide T/SP made by SOLARONIXS was applied by a screen printing method using a printing plate in which 18 patterns each having 180 mm length and 9 mm width had been produced at intervals of 1 mm on a polyester 27 mesh, and dried at 100 degrees C. The substrate to which the application had been made was burned at 500 degrees C for 30 minutes. The film thickness of the titania semiconductor layer after the burning was measured by a stylus film thickness gauge, and was found to be 12 μm. Next, after screen printing silver paste on 1 mm-width portions where titania had not been printed in widths of 0.5 mm and dried at 120 degrees C, burning was conducted at a heat treatment temperature of 550 degrees C for 10 minutes to produce a bus bar layer. The film thickness of obtained bus bar layer was 8 μm, and the result of resistivity measurement showed 5 μΩ.cm.

[0065]

After screen printing a glass paste material on this bus bar layer as a first protective layer 0.7 mm in width and drying for 120 degrees C, burning was performed at 550 degrees C for 10 minutes. This operation was repeated twice to produce the first protective layer. The resultant film thickness was 17 μm.

Next, after screen printing a polyimide resin material as a second protective layer at 0.7 mm in width and drying it at 100 degrees C, burning was performed under a nitrogen atmosphere at 400 degrees C for 60 minutes. The total film thickness of the bus bar layer, and the first and the second protective layers was 35 μm.

The resultant substrate was soaked in ruthenium dye/ethanol solution (3.0 × 10-4 mol/L) indicated by the following expression (1) for 15 hours to make the dye be adsorbed.

Furthermore, as a catalyst electrode substrate, film formation of Pt was carried out on a titanium board of 20 cm square with a film thickness of 30 nm.

[0066]

The titania electrode substrate and the catalyst electrode substrate produced as such were made to be opposite each other having a distance of 50 μm, the whole periphery portions between the substrates were bonded using a seal agent, and a cell of 20 × 20 cm size having an electrolyte solution inlet in a cell surface, but not in a cell cross-section, was assembled.

Next, as an electrolyte, methoxypropionitrile electrolyte solution including lithium iodide of 0.5 mol/L, iodine of 0.05 mol/L, and 4-t-butylpyridine of 0.5 mol/L is injected in the cells by a vacuum injection method, and the inlet was sealed.

By repeating the above-mentioned operations, five 20 cm-square cells were produced.

Artificial solar light of AM1.5G was irradiated to the cells obtained in this way, and a current-voltage property was measured. The result is indicated in Table 1.

The fluctuation range of the solar cell performance (conversion efficiency) of the five produced cells was 0.3%."

Consequently, Cited Document 5 discloses "a technical matter to screen print a polyimide resin material of 0.7 mm in width" (hereinafter, referred to as "the technical matter of Cited Document 5").

(3) Cited Document 6

Japanese Unexamined Patent Application Publication No. 2003-298078 (hereinafter, referred to as "Cited Document 6") which was cited in the Reasons for Refusal, the Decision of Refusal, and the Reconsideration Report, and had been distributed in advance of the priority date of the present application, shows the following matters. (The underlines are added by the body.)

(a) "[0001]
[Technical Field] The present invention relates to a photovoltaic power element such as a back-contact solar cell having a PN junction and positive and negative electrodes aligned on a surface opposite a light incident surface."

(b) "[0021] Next, with reference to FIG. 6, description will be given on a method of fabricating a photovoltaic power element of the present invention. First, as shown in FIG. 6(a), a substrate 11 of an N-type single crystal or a polycrystal silicon is prepared. As described above, a dendritic web crystal or a ribbon polycrystal can be used for this. Then, cleaning is performed to remove an oxidized film and the like adhered on the surface, and the surface is made to be a clean state. Next, as shown in FIG. 6(b), amorphous intrinsic silicon films 12 and 20 are formed on each of the front and rear faces of the substrate 11, respectively, by catalyst CVD. Although it is preferred that this thickness be equal to or more than 0.1 nm and equal to or less than 50 nm, they are formed with about 10 nm thickness as an example. An example of forming conditions of this amorphous intrinsic silicon film is as stated below.
Gas flow volume: SiH4 = 20 sccm
Gas ratio: SiH4/H2 = 1: 10

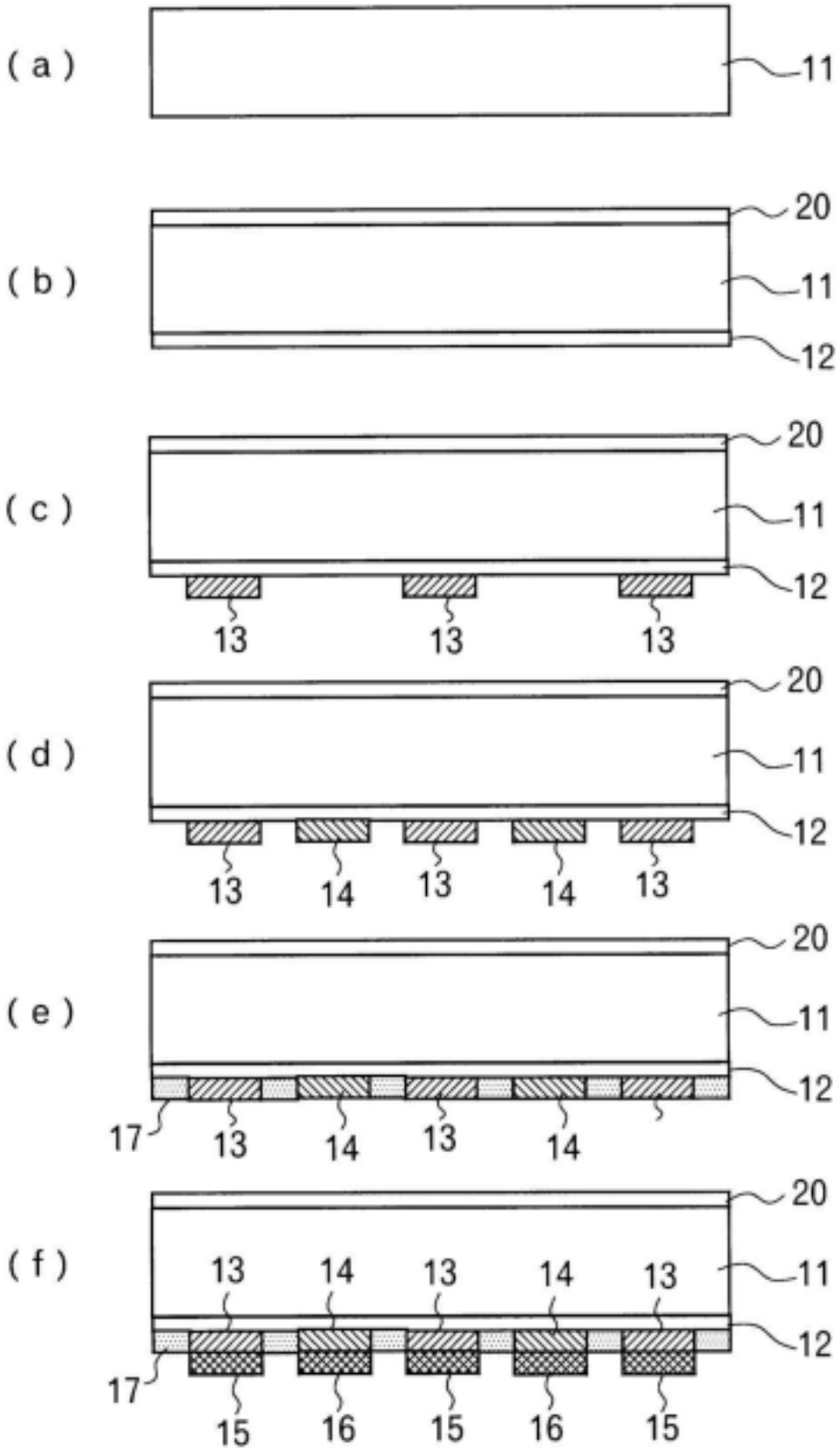
Film formation pressure: 1 Pa
Substrate temperature: 250 degrees C
Filament temperature: 1800 degrees C

[0022] Next, as shown in FIG. 6(c), an amorphous conductive silicon layer 13 is formed by catalyst CVD. Here, the conductive silicon layer 13 is a P-type, and the film thickness is made to be about 30 nm, for example. This P-type amorphous silicon layer is formed under:
gas flow volume: SiH_4 = 20 sccm, B_2H_6 = 1 sccm (1%, H_2 dilution),
gas ratio: SiH_4/H_2 = 1: 10,
film formation pressure: 1 Pa,
substrate temperature: 250 degrees C, and
filament temperature: 1800 degrees C.

[0023] Next, as shown in FIG. 6(d), an amorphous conductive silicon layer 14 of N-type is formed. Using a metal mask in a similar fashion, multiple parallel patterns are formed in a manner being inserted between pieces of conductive silicon layer 13 in a comb-teeth shape. The film thickness is around 30 nm, for example. The conditions of the formation are:
gas flow volume: SiH4 = 20 sccm, PH3 = 1 sccm (1%, H_2 dilution),
gas ratio: SiH_4/H_2 = 1: 10,
film formation pressure: 1 Pa,
substrate temperature: 250 degrees C, and
filament temperature: 1800 degrees C.

[0024] Next, as shown in FIG. 6(e), a protective film 17 is formed. The protective film 17 is formed, for example, by embedding polyimide resin paste between the conductive silicon layers 13 and 14 by a screen printing method and the like, and applying heat at a temperature of 250 degrees C or less to harden it. By formation of this protective film 17, weather resistance and soldering resistance are improved. Then, as shown in FIG. 6(f), by applying silver paste by screen printing, for example, and heating this at a relatively low temperature of 250 degrees C or less in a similar fashion to harden it, electrode patterns 15, 16, 15a, and 16a shown in FIG. 3 of a comb-teeth shape inserted between each other are formed."

(c) "[FIG. 6]


(a)
11
(b)
20
11
12
(c)
20
11
12
13
13
13
(d)
20
11
12
13
14
13
14
13
(e)
20
11
12
17
13
14
13
14
(f)
20
13
14
13
14
13
11
12
17
15
16
15
16
15

"

Consequently, the above-mentioned Cited Document 6 discloses "a technical matter to form polyimide resin paste by a screen printing method and the like" (hereinafter, referred to as "the technical matter of Cited Document 6").

(4) Comparison

The Amended Invention 8 is compared with the Cited Invention.

(a) "The n-doped region 14 and the p-doped region 16," "the substrate 10," "the first and second protective layers 18 and 20," "the first insulator layer 26a," and "the method of fabricating solar cell" of the Cited Invention respectively correspond to "the plurality of diffusion regions," "the solar cell wafer," "the first dielectric layer," "the second dielectric layer," and "the method of fabricating a solar cell" of the Amended Invention 8.

(b) "The substrate 10" of the Cited Invention in which "by making dopants of the doped glasses 36 and 40 to be diffused into the surface of the substrate 10 to form the n-doped region 14 and the p-doped region 16" and "a solar cell wafer having a plurality of diffusion regions adjacent to each other" of the Amended Invention 8 are common in a point of being "a solar cell wafer having a plurality of diffusion regions."

(c) The structure of the Cited Invention that "the first protective layer 18 made of oxidized silicon is formed on the substrate 10, and, along with this, the second protective layer 20 made of silicon nitride is formed over the first protective layer 18" corresponds to "forming the first dielectric layer on a solar cell wafer" of the Amended Invention 8.

(d) "The first insulator layer 26a" of the Cited Invention is one that is formed by "piercing the opened windows 34 into the first and second passivating layers 18 and 20 to expose the surface of the substrate 10; sticking the phosphorus-doped glass 36 to the second passivating layer 20 to fill the opened windows 34; between the first-pierced opened windows 34 of the first group, piercing the opened windows 38 of the second group, respectively; sticking the boron-doped glass 40 to the surface of the substrate 10 to fill the opened windows 38 of the second group; making dopants in the doped glasses 36 and 40 to be diffused into the surface of the substrate 10 to form the n-doped region 14 and the p-doped region 16; removing all of the glasses 36 and

40 on the substrate surface; after the first metal layer 24 is deposited, conducting patterning and etching such that all of the doped regions 14 and 16 have separate setting; sticking the first insulator layer 26a made of polyimide on the first metal layer 24; conducting patterning to the first insulator layer 26a to pierce a plurality of the opened windows 44," and, thus, it is obvious that a plurality of the first insulator layer 26a are formed on "the first and second passivating layers 18 and 20" between first metal layer 24 to which patterning has been conducted. Therefore, the structure to form "the first insulator layer 26a" by "piercing the opened windows 34 into the first and second passivating layers 18 and 20 to expose the surface of the substrate 10; sticking the phosphorus-doped glass 36 to the second passivating layer 20, and filling the glass 36 into the opened windows 34; between the first-pieced opened windows 34 of the first group, piercing the opened windows 38 of the second group, respectively; sticking the boron-doped glass 40 to the surface of the substrate 10, and filling the glass 40 into the opened windows 38 of the second group; making dopants of the doped glasses 36 and 40 to be diffused into the surface of the substrate 10 to form the n-doped region 14 and the p-doped region 16; removing all the glasses 36 and 40 on the substrate surface; after depositing the first metal layer 24, conducting patterning and etching such that all of the doped regions 14 and 16 have separate setting; sticking the first insulator layer 26a made of polyimide to the first metal layer 24; and conducting patterning to the first insulator layer 26a to pierce a plurality of opened windows 44" corresponds to the structure of the Amended Invention 8 of "forming a plurality of second dielectric layers" " over the first dielectric layer."

In addition, "the plurality of opened windows 44" of the above-mentioned Cited Invention that have been "pierced" in "the first insulator layer 26a" formed multiply correspond to "an opening between dielectric layers" "of a plurality of second dielectric layers" of the Amended Invention 8.

(e) In the Cited Invention, it is obvious that "a photoresist film" is formed after forming "the first insulator layer 26a," and it is also obvious that the "photoresist film" has an opening for "piercing the opened windows 44" into "the first insulator layer 26a."

In addition, it is obvious that "a plurality of dots" of the Amended Invention 8 is formed after forming "the second dielectric layer."

Therefore, the structure of the Cited Invention of "the first insulator layer 26a is patterned to pierce the opened windows 44, and, more specifically, a thin film of photoresist is formed on the polyimide layer 26, making the photoresist film be

exposed to ultraviolet light through a photolithography mask, developing the photoresist film using a developer, and etching the polyimide to pierce the plurality of opened windows 44," and the structure of the Amended Invention 8 of "printing a plurality of dots at least in an opening between two of the dielectric layers, the plurality of dots forming a contact mask that forms a plurality of gaps having a smaller area than an area of the plurality of dots, each of the gaps being defined by intersections of overlapping dots in the plurality of dots" are common in a point of forming a contact mask having a plurality of gaps after forming "the second dielectric layer."

(f) The structure of the Cited Invention of "piercing the opened windows 34 into the first and second passivating layers 18 and 20 to expose the surface of the substrate 10," and "between the first-pierced opened windows 34 of the first group, piercing the opened windows 38 of the second group, respectively" and the structure of the Amended Invention 8 of "etching portions of the first dielectric layer exposed through the gaps to form a plurality of contact regions exposing a plurality of diffusion regions of the solar cell" are identical in "etching a plurality of portions of the first dielectric layer to form a plurality of contact areas."

(5) Corresponding feature

Consequently, the Amended Invention 8 and the Cited Invention are identical in the following viewpoint:

"a method of fabricating solar cell, comprising:

forming a first dielectric layer on a solar cell wafer;

forming a plurality of second dielectric layers over the first dielectric layer;

forming a contact mask having a plurality of gaps after forming the second dielectric layers; and

etching a plurality of portions of the first dielectric layer to form a plurality of contact areas,

wherein the solar cell wafer has a plurality of diffusion regions, and a plurality of openings are provided between the plurality of second dielectric layers".

However, there are differences in the following features.

(6) The different features

(a) The different feature 1

In the Amended Invention 8, "a first dielectric layer is formed on a solar cell wafer having diffusion regions adjacent to each other" while in the Cited Invention "the

n-doped region 14 and the p-doped region 16" are formed after forming "the first and second passivating layers 18 and 20," and, in addition, "the n-doped region 14 and the p-doped region 16" aren't contiguous to each other.

(b) The different feature 2

In the Amended Invention 8, "a plurality of second dielectric layers are formed over the first dielectric layer and on a boundary between an adjacent pairs of the diffusion regions" while in the Cited Invention, although a plurality of "the first insulator layer 26a" are formed on "the first and second passivating layers 18 and 20," they not located on the boundary between "the n-doped region 14 and the p-doped region 16."

(c) The different feature 3

In the Amended Invention 8, "a plurality of dots are printed" and "the plurality of dots forming a contact mask that forms a plurality of gaps having a smaller area than an area of the plurality of dots, each of the gaps being defined by intersections of overlapping dots in the plurality of dots," and "the plurality of dots" are printed "in at least an opening between two of the second dielectric layers" while in the Cited Invention, the film-forming method of a "photoresist film" is unclear, and how an opening for "piercing the opened windows 44" of the "photoresist film" is formed is unclear, there is no statement of "a plurality of dots" in the Cited Invention, and, therefore, whether or not "a plurality of dots" are formed in "at least a plurality of openings between the plurality of second dielectric layers" is undefined.

(d) The different feature 4

In the Amended Invention 8, "etching a plurality of portions of the first dielectric layer exposed through the gaps to form a plurality of contact regions exposing a plurality of diffusion regions of the solar cell" while in the Cited Invention "the opened windows 34 is pierced into the first and second passivating layers 18 and 20 to expose the surface of the substrate 10" and, thus, no diffusion region is exposed.

(7) Judgment

(a) Regarding the different feature 1, the different feature 2, and the different feature 4

In the Cited Invention, a person skilled in the art can decide whether diffusion regions are formed contiguously or they are spaced depending on his/her preference.

In this case, "the first insulator layer 26a" positioned between "the first metal layer 24" to which "pattern processing and etching processing is performed such that each of the doped regions 14 and 16 has an independent setting" will be located on the boundary between "the doped regions 14 and 16," and, therefore, it could have easily derived by a person skilled in the art to embody the above-mentioned different feature 2 in the Cited Invention.

However, the Cited Invention is one "forming the first passivating layer 18 made of oxidized silicon on the substrate 10, forming the second passivating layer 20 made of silicon nitride over the first passivating layer 18, piercing the opened windows 34 into the first and second passivating layers 18 and 20 to expose the surface of the substrate 10, and sticking the phosphorus-doped glass 36 to the second passivating layer 20 to fill the opened windows 34;

between the first-pierced opened windows 34 of the first group, piercing the opened windows 38 of the second group, respectively, sticking the boron-doped glass 40 to the surface of the substrate 10 to fill the glass 40 in the opened windows 38 of the second group, making dopants of the doped glasses 36 and 40 be diffused into the surface of the substrate 10 to form the n-doped region 14 and the p-doped region 16," and, in the Cited Document 1, there is no statement or suggestion to, in place of the structure of the above-mentioned Cited Invention, make it be of a structure of "forming a first passivating layer 18 made of oxidized silicon on a substrate 10, forming a second passivating layer 20 made of silicon nitride over the first passivating layer 18," the substrate 10 having "the n-doped region 14 and the p-doped region 16 formed thereon." In addition, also in Cited Documents 2 to 6, there is no statement of "a first dielectric layer is formed on a solar cell wafer having a plurality of diffusion regions adjacent to each other." Consequently, it could not have easily derived to embody the above-mentioned different feature 1 in the Cited Invention,.

For that reason, in the Cited Invention, also to embody "the n-doped region 14 and the p-doped region 16" being exposed by "piercing the opened windows 34 into the first and second passivating layers 18 and 20 and exposing the surface of the substrate 10"; that is, the structure relating to the above-mentioned different feature 4, could not have been easily derived.

Accordingly, even based on the technical matters disclosed in the Cited Invention, the well-known art of Cited Documents 2 to 3, and the well-known art disclosed in Cited Document 4, and, the technique to screen print a polyimide resin material that is a technical matter of the above-mentioned Cited Documents 5 to 6, the structure relating to the above-mentioned different feature 1 and the different feature

4 cannot be obtained.

(b) About the different feature 3

The different feature 3 is similar to the different feature that has been explained in "(7)" regarding the Amended Invention 1." Thus, also regarding the different feature 3, like the judgment that has been explained in "(8)" regarding the Amended Invention 1, the structure relating to the different feature 3 cannot be obtained on the basis of the Cited Invention, the well-known technique disclosed in Cited Documents 2 to 3, and the well-known art disclosed in Cited Document 4.

In addition, even on the basis of the technique to screen print a polyimide resin material that is a disclosed in the above-mentioned Cited Documents 5 to 6, the structure relating to the different feature 3 cannot be obtained.

Therefore, even on the basis of the Cited Invention, the well-known art described in Cited Documents 2 to 3, the well-known art described in Cited Document 4, and the technique to screen print a polyimide resin material that is disclosed in the above-mentioned Cited Documents 5 to 6, the structure relating to the above-mentioned different feature 3 cannot be obtained.

(8) Conclusion

Consequently, since it can be denied that the Amended Invention 8 could have been easily invented by a person skilled in the art on the basis of the Cited Invention, the well-known art disclosed in Cited Documents 2 to 3, the well-known art disclosed in Cited Document 4, and the technical matters disclosed in Cited Documents 5 to 6, and it can be denied that the Amended Invention 8 cannot obtain a patent in accordance with the provisions of Article 29(2) of the Patent Act.

In addition, beyond that, there is no other reason to deny their patentability.

4. About the Amended Inventions 9 and 10

Since The Amended Inventions 9 and 10 contain all of the subject matters of the invention of the Amended Invention 8, it can be denied that they could have been easily invented by a person skilled in the art ,like the Amended Invention 8, on the basis of the Cited Invention, the well-known art disclosed in Cited Documents 2 to 3, the well-known art disclosed in Cited Document 4, and the technical matters disclosed in Cited Documents 5 to 6, and it can be denied that the Amended Inventions 9 and 10 cannot obtain a patent in accordance with the provisions of Article 29(2) of the Patent Act.

In addition, beyond that, there is no other reason to deny their patentability.

5. Summary

As mentioned above, it cannot be accepted that the appellant should not be granted a patent as for the Amended Inventions 1 to 10 in accordance with the provisions of Article 29(2) of the Patent Act as reported in the Reconsideration Report, and, beyond that, there is no other reason to deny their patentability.

Therefore, it cannot be accepted that it should be dismissed under the provisions of Article 53(1) of the Patent Act as applied mutatis mutandis pursuant to the provisions of Article 159(1) of the Patent Act with relevant changes in interpretation on the grounds that the Amendment of the case violates the provisions of Article 126(5) of the Patent Act as applied mutatis mutandis pursuant to the provisions of Article 17-2(5) of the Patent Act.

No. 3 About the Decision of Refusal

Whether or not the present application should be rejected due to the reason of the Decision of Refusal is taken into consideration.

As mentioned above, since it cannot be accepted that the Amendment of the case should be dismissed, the inventions according to claims 1 to 10 of the scope of claims of the present application are the Amended Inventions 1 to 10.

Then, as mentioned above, the Amended Inventions 1 to 7 could not have been easily invented by a person skilled in the art on the basis of the Cited Invention and the technical matters disclosed Cited Documents 2 to 4, and, in addition, the Amended Inventions 8 to 10 could not have been easily invented by a person skilled in the art on the basis of the Cited Invention, and the technical matters disclosed Cited Documents 2 to 6. Therefore, it cannot be accepted that the appellant should not be granted a patent for the Amended Inventions 1 to 10 in accordance with the provisions of Article 29(2) of the Patent act, and, consequently, it cannot be accepted that the present application shall be rejected due to the reason of the Decision of Refusal.

No. 4 Conclusion

Accordingly, regarding the present application, taking into consideration the Reasons for Refusal of the original decision, it cannot be accepted that it shall be refused on the basis of those reasons.

In addition, beyond that, there is no other reason for refusal.
Therefore, the appeal decision shall be made as described in the conclusion.

Jun. 24, 2015

Chief administrative judge: ITO, Masaya
Administrative judge: YAMAGUCHI, Tsuyoshi
Administrative judge: JIN, Yoshihiko