Appeal Decision

Appeal No. 2014- 20849

USA
Appellant MICRON TECHNOLOGY INC.

Tokyo, Japan
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The case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2011-542905, "Enhanced Addressability for Serial Non-volatile Memory" (PCT International Publication: WO2010/076600 published on July 8, 2010, Domestic Publication of PCT International Patent Application: No. 2012-514247 published on June 21, 2012, Number of claims: 14) has resulted in the following appeal decision.

Conclusion

The examiner's decision is revoked.

The Invention of the present application shall be granted a patent.

Reasons

No. 1 History of the procedures

The application was originally filed on December 30, 2008 as an International Patent Application, and the history of the procedures is as follows:

August 26, 2011	Submission of the translation
April 19, 2013	Notice of the reasons for refusal (drafting date)
July 29, 2013	Submission of the written opinion and written amendment
November 28, 2013	Notice of the reasons for refusal (final reasons for refusal) (drafting date)
February 25, 2014	Submission of the written opinion and written amendment

June 12, 2014	Decision to dismiss the amendment submitted on February. 25, 2014, Decision of refusal (drafting date)
October 15, 2014	Submission of the request for appeal and written amendment

No. 2 Invention

The inventions according to claims 1 to 14 of the application are acknowledged as follows, as specified by the matters described in claims 1 to 14 amended by the written amendment dated on October 15, 2014:

"[Claim 1]

A serial non-volatile memory device, comprising:

a plurality of storage locations organized into a plurality of banks;

an extended address register that stores an extended address value to identify a first bank of the plurality of banks;

an input terminal through which the extended address value, a high-speed Read command associated with processing of reading a contiguous block of data items from the non-volatile memory device, and an address are received; and

a control unit to access data items of contiguous banks by beginning at a storage location identified by a combined address comprising the extended address value stored in the extended address register and the address, and spanning a border between the first bank of the plurality of banks and a second bank of the plurality of banks by incrementing the combined address.

[Claim 2]

The memory device according to claim 1, wherein the extended address value includes an 8-bit value.

[Claim 3]

The memory device according to claim 2, wherein the address includes a 24-bit address.

[Claim 4]

The memory device according to claim 3, wherein the control unit is adapted to perform a Read and/or Write operation compatible with a serial peripheral interface protocol, and the serial non-volatile memory device includes a serial flash memory device.

[Claim 5]

The memory device according to claim 4, wherein the control unit is further adapted to perform a Write operation, which is compatible with the serial peripheral

interface protocol, on the extended address register at least in part in response to receiving of the extended address value through the input terminal.

[Claim 6]

The memory device according to claim 1, wherein one or more of the plurality of banks has 16M (mega) storage locations.

[Claim 7]

The memory device according to claim 6, wherein one or more of the plurality of storage locations includes an 8-bit storage location, and the plurality of banks include a bank having a capacity of 128 Mb so as to provide a total capacity large enough for the memory device having a storage capacity larger than 128 Mb.

[Claim 8]

A system comprising:

a processor; and

a serial non-volatile memory device that is connected to the processor, wherein

the memory device includes

a plurality of storage locations organized into a plurality of banks;

an extended address register that stores an extended address value to identify a first bank of the plurality of banks;

an input terminal through which the extended address value, a high-speed Read command associated with processing of reading a contiguous block of data from the non-volatile memory device, and an address are received from the processor; and

a control unit to access data items of contiguous banks by beginning at a storage location identified by a combined address comprising the extended address value stored in the extended address register and the address, and spanning a border between the first bank of the plurality of banks and a second bank of the plurality of banks by incrementing the combined address.

[Claim 9]

The system according to claim 8, wherein the extended address value includes an 8-bit value.

[Claim 10]

The system according to claim 9, wherein the address includes a 24-bit address.

[Claim 11]

The system according to claim 8, wherein the control unit is adapted to perform a Read and/or Write operation compatible with a serial peripheral interface protocol, and the serial non-volatile memory device includes a serial flash memory device.

[Claim 12]

The system according to claim 11, wherein the control unit is further adapted to perform a Write operation, which is compatible with the serial peripheral interface protocol, on the extended address register at least in part in response to receiving of the extended address value from the processor.

[Claim 13]

The system according to claim 8, wherein one or more of the plurality of banks includes 16M (mega) storage locations.

[Claim 14]

The system according to claim 13, wherein one or more of the plurality of storage locations includes an 8-bit storage location, and the plurality of banks includes a bank having a capacity of 128 Mb so as to provide a total capacity large enough for the memory device having a storage capacity larger than 128 Mb."

No. 3 Outline of reasons for refusal stated in the examiner's decision

Among the reasons of the examiner's decision, outline of the reason for rejection of claim 1 is as follows:

The invention according to the claim below of the present application cannot be granted a patent under the Article 29(2) of the Patent Act because the invention could be easily made by a person ordinarily skilled in the field of the art, to which the invention belongs, prior to the application on the basis of the inventions described in the publications below distributed in Japan or abroad prior to the application or an invention that is made available to public over an electric communication network.

Note (Refer to the List of Cited documents regarding Cited Documents, etc.)

- Claim 1
- Cited Documents 1 and 2
- Remarks

Referring to paragraphs [0029]to[0036] and Fig. 3 of Cited Document 1, the Cited Document 1 describes a flash memory 200 (equivalent to a "non-volatile memory" in the Invention) in which an access location is determined with bit data items A0 to A15 of an address signal (A0 to A13 are equivalent to an "address" in the Invention, A14 and A15 are equivalent to an "extended address value" in the Invention, and A0 to A15 are equivalent to a "combined address" in the Invention), and access is gained to one of flash memory chips 220 to 223 (equivalent to a "plurality of subsets" in the Invention) that stores an extended address value, which is consistent with an

extended address value specified with the bit data items A14 and A15 of the address signal, in a register part of the flash memory chip. It is a matter of common practice that, when comparison is made in order to decide whether the addresses are consistent with each other, the address that is an object of comparison is preserved in the register. Therefore, it is a matter, which should be properly designed by a person skilled in the art, from the invention described in the Cited Document 1, to arrange that the extended address value specified with the bit data items A14 and A15 of the address signal is preserved in a register.

The Cited Document 1 does not describe that access is gained to data items of blocks which adjoin across a border between a plurality of flash memory chips. However, a high-speed read technology of designating as an access area a contiguous area within a predetermined range while beginning with a predetermined start address, and then sequentially accessing the designated access area is already well known (for example, paragraphs [0028] to[0037] in Cited Document 2). Therefore, it is a matter, which could be easily made by a person skilled in the art, that the above well-known art is applied to the invention described in the Cited Document 1 in order to make it possible to designate as an access area a contiguous area across the border of two of the flash memory chips 220 to 223, and then to access the contiguous block of data items across the border between two of the plurality of flash memory chips.

The other points are matters which should be properly designed by a person skilled in the art.

Therefore, the invention according to claim 1 of the application could be easily made by a person skilled in the art on the basis of the Cited Document 1 and well-known art.

List of Cited Documents, etc.

1. Japanese Unexamined Patent Application Publication No. 2000-3305
2. Japanese Unexamined Patent Application Publication No. 2008-9874

No. 4 Judgment by the body

1. Invention according to claim 1 (hereinafter, the Invention 1)

(1) Cited Invention

The Cited Document 1 (Japanese Unexamined Patent Application Publication

No. 2000-3305) cited in the examiner's decision has the descriptions below (the underlines indicate points especially noted in the appeal decision).

"[0029] (2) Embodiment 2

A flash memory 200 in accordance with embodiment 2 will be described below. Fig. 3 is a configuration diagram of a system employing the flash memory 200. The flash memory 200 has four flash memory chips 220 to 223, which each have a storage capacity of 64 megabits and to which extended addresses (00, 01, 10, and 11) are assigned and address spaces (0 to 3FFFh, 4000 to 7FFFh, 8000 to BFFFh, and C000 to FFFFh) are allocated in order of the extended addresses, incorporated in one package. A control unit 150 of the system and the flash memory 200 are connected to each other over signal lines 151 and 152.

[0030] The control unit 150 outputs a chip enabling signal CE#, which has level L, over the signal line 152 so as to switch the flash memory 20 into an accessible state. Thereafter, the control unit 150 performs a sequence including outputting of a data Write or Read command over the signal line 151, outputting of an address signal of 2 bytes (16 bits) long which designates a sector address to be accessed within the address space 0 to FFFFh, and outputting of writing data or receiving of reading data. Note that # succeeding the symbol of the chip enabling signal indicates reversal of a signal level and signifies that the chips 220 to 223 are active-low. As described later, the flash memory 200 switches the chip, to which a sector address designated with an address signal is assigned, into an accessible state on the basis of the value of the address signal inputted from the system, without necessitating provision of another signal to be used to switch the state of a chip.

[0031] Fig. 4 is a configuration diagram of the flash memory 200. The flash memory 200 has four chips 220 to 223, which each have a storage capacity of 64 megabits, incorporated in it. The chips 220 to 223 have, in addition to the data storage areas, register parts 224 to 227 respectively, each of which is 1 byte long and stores an assigned extended address. As shown in Fig. 5, each of the chips 220 to 223 stores the assigned extended address value as 2-bit data of bit 0 and bit 1 in each of the register parts 224 to 227. The bit data items of bit 2 to bit 7 are ignored.

[0032] The chips 220 to 223 have address spaces (0 to 3FFFh, 4000 to 7FFFh, etc.) allocated to them in order of extended addresses (00, 01, etc.) stored in the register parts 224 to 227. To the chip 220, the extended address "00" is assigned and the address space 0 to 3FFFh is allocated. To the chip 221, the extended address "01" is assigned and the address space 4000 to 7FFFh is allocated. To the chip 222, the extended

address "10" is assigned and the address space 8000 to BFFFh is allocated. To the chip 223, the extended address "11" is assigned and the address space C000 to FFFFh is allocated.

[0033] An operating voltage Vcc and a predetermined signal such as a reset signal RES# are inputted to the four chips 220, 221, 222, and 223 through pins 201 to 205 and 214 to 216 disposed on the flank of the package of the flash memory 200. In addition, a data Write or Read command, an address signal of 2 bytes (16 bits) long designating a sector address to be accessed, and writing data or reading data are transferred through the pins 206 to 213 to which terminals I/O0 to I/O7 are assigned.

[0034] The address signal is data of 16 bits long (A0 to A15) comprising SA1 and SA2, each of which is 1 byte long, and takes on a value ranging from 0 to FFFFh. The association of the signals SA1 and SA2, which are inputted in parallel with each other in units of 1 byte through the terminals I/O0 to I/O7, with the data of 16 bits (A0 to A15) long that are used to designate the sector address is identical to the one in Table 1.

[0035] The assigned pins 212 and 213 of the terminals I/O6 and I/O7 are connected to extended address input terminals 234, 235, 236, 237, 238, 239, 240, and 241 of the chips 220 to 223. A chip enabling terminal 228 is connected to chip enabling terminals 230 to 233 of the chips 220 to 223 respectively.

[0036] The chip enabling signal CE# of level L is inputted to the chips 220 to 223 through the chip enabling terminal 228 of the flash memory 200. Only when the extended address value (A15, A14) specified with the bit data items A14 and A15 of the address signal inputted through the extended address input terminals (234, 235, 236, 237, 238, 239, 240, and 241) is consistent with the extended address assigned to any of the chips 220 to 223, the chip is switched to an accessible state. By adopting the configuration, the necessity of the decoder 121 employed in the flash memory 100 of the embodiment 1 can be obviated and the internal configuration can be simplified. "

When the above descriptions in the Cited Document 1 are collated with relevant Figs. 3 to 5 of the Cited Document 1, and the common general technical knowledge, paying attention to the underlined parts, it can be said that the invention below (hereinafter, Cited Invention) is described in the Cited Document 1.

"A flash memory 200 comprising:

a plurality of storage addresses formed with a plurality of chips 220 to 223;

register parts 224 to 227 that each store an extended address value with which one of the chips 220 to 223 is identified; and

input terminals I/O0 to I/O7 through which a Read command associated with processing of reading data from the flash memory 200 and an address are received."

(2) Comparison

By comparing the Invention 1 with the Cited Invention, a description can be made as follows:

A. The "plurality of chips 220 to 223" and "plurality of storage addresses" in the Cited Invention are equivalent to the "plurality of banks" and "plurality of storage locations" in the Invention 1.

B. "One chip," "an extended address value," and "register parts 224 to 227" in the Cited Invention are equivalent to the "first bank," "extended address value," and "extended address register" in the Invention 1.

C. The "flash memory 200," "address," and "input terminals I/O0 to I/O7" in the Cited Invention are equivalent to the "non-volatile memory device," "address," and "input terminal" in the Invention 1. The "Read command associated with processing of reading data" in the Cited Invention and the "high-speed Read command associated with processing of reading data items of adjoining blocks" in the Invention 1 correspond to each other in terms of a "Read command associated with processing of reading data."

Therefore, it can be said that the Invention 1 and Cited Invention have corresponding features and different features described below.

(Corresponding features)

"A non-volatile memory device comprising:

a plurality of storage locations organized into a plurality of banks;

an extended address register that stores an extended address value with which a first bank of the plurality of banks is identified; and

an input terminal through which a Read command associated with processing of reading data from the non-volatile memory device and an address are received. "

(Different feature 1)

In the Invention 1, an "extended address value" is "received" through an "input terminal." In contrast, the Cited Invention does not have an equivalent configuration.

(Different feature 2)

The Invention 1 receives "a high-speed Read command associated with

processing of reading a contiguous block of data from the non-volatile memory device," and includes a "control unit to access data items of contiguous banks by beginning at a storage location identified by a combined address comprising the extended address value stored in the extended address register and the address, and spanning a border between the first bank of the plurality of banks and a second bank of the plurality of banks by incrementing the combined address." In contrast, the Cited Invention does not have an equivalent configuration.

(3) Judgment

A. (Regarding the different feature 1)

How to acquire an extended address value, which is stored in any of the register parts 224 to 227, in the Cited Invention is a mere design-related matter or a matter to be properly designed by a person skilled in the art at the time of implementation. The configuration that the extended address value is externally acquired through the input terminals I/O0 to I/O7 in the Cited Invention could be easily made by the person skilled in the art.

B. (Regarding the different feature 2)

In consideration of the descriptions in the publication No. 2008-9874 cited in the examiner's decision and Japanese Unexamined Patent Application Publications Nos. 11-120075 and 5-274215 cited in the reconsideration report, the body has judged that it cannot be said to be easy for the Cited Invention to overcome the different feature 2.

The reasons are as follows:

(A) The Invention 1 employs a combined address comprising an extended address value (8 bits of bits 31 to 24 in Fig. 4 of the Invention, or 8 high-order bits) stored in an extended address register (extended address register 224 in Figs. 1 and 4 of the Invention) and an address (24-bit address 402 of bits 23 to 0 in Fig. 4 of the Invention, or 24 low-order bits).

In contrast, the Cited Document 1 does not describe that a combined address is formed using an extended address value (A15 and A14) stored in any of the register parts 224 to 227 and an address (A0 to A13) inputted through the terminals I/O0 to I/O7. The Cited Document 1 describes that A0 to A15 are always externally received for a Read command but does not describe a technical idea of producing a combined address that includes high-order bits and low-order bits.

(B) The publication No. 2008-9874 cited in the examiner's decision (refer to paragraphs [0028] to [0037] and Fig. 4), Japanese Unexamined Patent Application Publication No. 11-120075 (refer to paragraphs [0074] to [0077] and Fig. 9), and Japanese Unexamined Patent Application Publication No. 5-274215 (refer to paragraphs [0013] to [0023] and Fig. 1) cited in the reconsideration report describe a well-known art of performing high-speed reading spanning a border between contiguous physical blocks or physical chips (equivalent to banks in the application) by incrementing an address.

However, the constituent feature relating to the different feature 2 of the application "To access data items of contiguous banks by beginning at a storage location identified by a combined address comprising the extended address value stored in the extended address register and the address, and spanning a border between the first bank of the plurality of banks and the second bank of the plurality of banks by incrementing the combined address " cannot be deduced from the Cited Invention and well-known art.

Therefore, it cannot be said to be easy for the Cited Invention to overcome the different features.

2. Inventions according to claims 2 to 14

The invention according to claim 8 (hereinafter, the Invention 8) is an invention of a "system" including the constituent components of the Invention 1, and the inventions according to claims 2 to 7 and 9 to 14 further limit the Invention 1 or the Invention 8. Therefore, it cannot be said that the inventions could, similarly to the Invention 1, be easily made based on the Cited Invention by a person skilled in the art.

No. 5 Closing

As described so far, the inventions according to claims 1 to 14 of the application could not be easily made based on the Cited Invention by a person skilled in the art. Therefore, the application cannot be rejected due to the reasons of the examiner's decision.

In addition, beyond that, no reasons for refusal were found.

Therefore, the appeal decision shall be made as described in the conclusion.

October 14, 2015

Chief administrative judge: KOBIKI, Mitsuaki
Administrative judge: SAKURAI, Shigeyuki
Administrative judge: CHIBA, Teruhisa