Appeal Decision

Appeal No. 2014-22371

Singapore
Appellant KINGLITE HOLDINGS INC.

Tokyo, Japan
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The case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2013-17748, entitled "Method and Apparatus for Providing Intelligent Power Management" (the application published on June 13, 2013, Japanese Unexamined Patent Application Publication No. 2013-117981) has resulted in the following appeal decision:

Conclusion

The appeal of the case was groundless.

Reason

1. History of the procedures

The present application is a divisional application filed on January 31, 2013 from Patent Application No. 2000-580071 filed on November 4, 1999 as an international filing date (priority claim under the Paris Convention, received by the foreign receiving office, November 4, 1998, the US), and a written amendment was submitted at the same time. Then, reasons for refusal were notified on October 11, 2013 and a written amendment was submitted on January 22, 2014; however, the examiner's decision of refusal was issued on June 25, 2014. Against this, an appeal against the examiner's decision of refusal was requested on November 4, 2014.

2. The Invention

The invention according to Claim 8 of the present application (hereinafter referred to as "the Invention") is acknowledged as follows, as described in Claim 8 in the written amendment dated January 22, 2014:

"[Claim 8]

A power management method for a circuit in a processor-based system, comprising:

(a) using an instruction sequence executed separately from an application program which uses the circuit, and determining an operation mode corresponding to the type of the application program of the circuit; and

(b) in response to the operation mode, operating the circuit at a first predetermined speed or operating the circuit at a second predetermined speed higher than the first predetermined speed."

3. Cited Invention

Japanese Unexamined Patent Application Publication No. H5-241677 (hereinafter, referred to as "the Cited Document") that was cited in the reasons for refusal of the examiner's decision includes the following description:

"[Detailed Description of the Invention]
[0001]
[Industrial Application Field]
This invention relates to a personal computer, more specifically, relates to managing battery power available in a portable computer by changing a clock frequency for computation in a central processing unit of a computer.
...
(Omitted)
...
[0012]
[Operation] This invention is to control a clock frequency at which an integrated circuit of a microprocessor operates, so as to reduce power consumption in low-speed calculation capability. That is, for example, during communication by a modem, a standby state in which a new instruction is not input, and other operations for executing ordinary simple calculation functions, the clock frequency is reduced to a lower operation frequency. In addition, for example, when more complicated calculation such as creating a display of a rotating 3D object, searching a large database, etc., is required, the clock frequency is increased to the maximum operation frequency. The number of instructions executed by a microprocessor per unit time increases along with an increase of the clock frequency and so, power consumption also increases along with the clock frequency. In addition, a thermal loss in the integrated circuit of the microprocessor also increases along with the clock frequency and as a result, a rise in the operation temperature occurs and the possibility of a failure tends to increase. Further, the rating of a mean time between failures (MTBF) accompanying them decreases.
[0013] The clock frequency generation circuit is connected to the microprocessor so as to supply a clock signal thereto and can continuously change the clock frequency within the range of conditions for stability of the clock signal which is supplied to the microprocessor so as to decrease or increase the clock frequency of the microprocessor according to a calculation condition. This ensures a proper operation of the microprocessor while continuously changing the clock frequency of the microprocessor between its upper limit and lower limit. By changing the frequency of the clock signal supplied to the microprocessor in this mode, the necessity to reset the microprocessor for operation at a specific new clock frequency is eliminated and in addition, continuous power management control according to calculation conditions is provided.
[0014]
[Examples]
FIG. 1 illustrates a schematic block diagram of a normal personal computer or workstation having a central processing unit 12 including a commercial microprocessor 13 such as the 80486 IC (commercially available from Intel Corporation). The central processing unit 12 can be controlled by a user via an input device 16 such as a keyboard, mouse, pen-type tablet, or the like; further a display device 14 for providing graphics or a text image 34, or a combination thereof in a known manner is included. The central

processing unit 12 can also be operated by input from a network 32 and data 20 can be stored in a memory 18 (and a large capacity storage device 30) for access and interaction by the central processing unit 12 in various calculation routines. All the central processing unit 12 and accompanying peripheral apparatuses can be supplied with power from the battery 33.

[0015] The speed of calculation operation or the number of instructions executed per second in the computer system in FIG. 1 is directly related to the frequency of a clock pulse supplied to the microprocessor 13 by the clock signal generation circuit 15. A commercially available microprocessor such as the 80486 IC generally requires a clock frequency which is specified within a narrow range. Therefore, such a microprocessor as above may require, for example, a clock frequency within the range from 16 to 33 MHz and may require, for example, a short-period stability of 0.1% or less in terms of variation between clock pulses.

[0016] The short-period stability of the clock pulse is generally important for, for example, allowing an internal phase-locked loop integrated in a microprocessor circuit to be locked on a stable clock pulse. The number of instructions executed per unit time increases in the microprocessor 13 having a high clock frequency and a thermal loss inside the microprocessor 13 also increases. Accordingly, the operation temperature rises, and available power of the battery 33 is exhausted further rapidly. Thus, it is preferable to reduce the frequency of a clock pulse supplied to the microprocessor 13 if possible so as to reduce the power consumption and operation temperature for extension of the battery life. However, a clock signal needs to be stable within a specified range and therefore, it is preferable that the clock frequency is changed by a sufficiently smaller increase or decrease than that for fully satisfying a short-term condition of clock pulse supply.

[0017] This allows the microprocessor 13 to continue its operation within a specification range and eliminates the necessity to reset the microprocessor with a newly fixed clock frequency. In addition, the clock frequency can be selected according to calculation conditions, for example, in such a manner that a low clock frequency is selected for low power consumption in a document processing program 24 and a large power consumption high clock frequency is selected for high-level calculation request such as a request to create a full-color display of a rotating 3D image 34.

...

(Omitted)

...

[0022] Accordingly, the system and method of the invention provide a technique that is useful to limit power consumption so that, by changing the frequency of a clock pulse supplied to the microprocessor, the speed of calculation or logical operation is reduced during calculation with low capability or the period of logical capacity (for example, by detecting nonoperation for a timeout period). When high-level calculation or logical operation is required (for example, when manual activation from the keyboard is performed or when an application program requiring a high-level or high-speed calculation capability is detected), the clock frequency can be increased as a continuous increase within an allowable limit specified for the stability of continuous clock intervals."

Considering the above description in the Cited Document in light of related drawings of the Cited Document and technical common sense, the following are recognized:

(1) According to descriptions in paragraphs [0001], [0015], etc., a method for managing battery power for the central processing unit 12 of a computer system shown in FIG. 1 is disclosed in the Cited Document.

(2) According to descriptions of paragraphs [0012], [0013], [0017], [0022], etc., it can be said that the "method" in the above (1) includes "a step for operating the central processing unit 12 at a specific low clock frequency according to the type of an application program (document processing program, high-level calculation request) of the central processing unit 12, or operating the central processing unit 12 at a specific high clock frequency that is higher than the specific low clock frequency."

In addition, the "specific low clock frequency" and "specific high clock frequency" of the above "step" specify the operation of the central processing unit 12 and therefore, it can be said to be operation modes (format, manner); and the above "step" naturally includes: "a step for determining an operation mode (a specific low clock frequency, specific high clock frequency) corresponding to the type of an application program (document processing program, high-level calculation request) of the central processing unit 12; and a step for, in response to the operation mode, operating the central processing unit 12 at a specific low clock frequency or for operating the central processing unit 12 at a specific high clock frequency higher than the specific low clock frequency."

Accordingly, it can be said that the "method" described in the above (1) includes "a step for determining an operation mode (a specific low clock frequency, specific high clock frequency) corresponding to the type of an application program (document processing program, high-level calculation request) of the central processing unit 12 and a step for, in response to the operation mode, operating the central processing unit 12 at a specific low clock frequency or for operating the central processing unit 12 at a specific high clock frequency higher than the specific low clock frequency."

Considering all of the above, it can be said that the following invention (hereinafter, referred to as "the Cited Invention") is described in the Cited Document:
"A method for managing battery power for a central processing unit 12 of a computer system comprising:

determining an operation mode corresponding to the type of an application program of the central processing unit 12; and

in response to the operation mode, operating the central processing unit 12 at a specific low clock frequency, or operating the central processing unit 12 at a specific high clock frequency higher than the specific low clock frequency."

4. Comparison

In comparison of the Invention and Cited Invention, the following are recognized:
(1) The "computer system" of the Cited Invention corresponds to the "processor-based system" of the Invention.

(2) The "central processing unit 12" of the Cited Invention corresponds to the "circuit" of the Invention.
(3) "Managing battery power" of the Cited Invention corresponds to the "power management" of the Invention.
(4) The "application program" of the Cited Invention corresponds to the "application program" of the Invention.
(5) The "specific low clock frequency" of the Cited Invention corresponds to the "first predetermined speed" of the Invention.
(6) The "specific high clock frequency higher ..." of the Cited Invention corresponds to the "second predetermined speed higher ..." of the Invention.

According to the above, there are the following corresponding and different features between the Invention and Cited invention.
(Corresponding features)
"A power management method for a circuit in a processor-based system, comprising:
determining an operation mode corresponding to the type of an application program of the circuit; and
in response to the operation mode, operating the circuit at a first predetermined speed or operating the circuit at a second predetermined speed higher than the first predetermined speed."

(Different feature)
"Determining an operation mode corresponding to the type of an application program of the circuit" in the Invention is described as "using an instruction sequence executed separately from an application program which uses the circuit, and determining an operation mode corresponding to the type of the application program of the circuit;" whereas, "determining an operation mode corresponding to the type of an application program (application program) of the circuit (the central processing unit 12)" in the Cited Invention is not described as "using an instruction sequence executed separately from an application program (application program) which uses the circuit (central processing unit 12), and determining an operation mode corresponding to the type of an application program (application program) of the circuit (central processing unit 12)."

5. Judgment
(1) Regarding the above description (the different feature)
Considering all of the following circumstances, it should be said that a person skilled in the art could have easily arrived at adopting the configuration of the Invention relating to the above different feature in the Cited Invention.
A. As is obvious from the descriptions of paragraphs [0017] and [0022], FIG. 1, etc. of the Cited Invention, it can be said that the "application program" of the Cited Invention is an "application program which uses the central processing unit 12."
B. Meanwhile, as shown in [Conventional Art], etc. of Japanese Unexamined Patent Application Publication No. H8-234876, it is a well-known art that a CPU (central processing unit) uses an instruction sequence called a power-saving program or power-saving application which is executed separately from an application program, so as to save power of the CPU (central processing unit); and there is no reason that the well-

known art cannot be adopted for the step of "determining an operation mode corresponding to the type of an application program of the central processing unit 12" in the Cited Invention.
C. In view of the above, a person skilled in the art could have easily conceived of adopting the above well-known art to the step of "determining an operation mode corresponding to the type of an application program of the central processing unit 12" in the Cited Invention.
D. The matters described above mean that a person skilled in the art could have easily adopted the configuration of the Invention relating to the above different feature, that is, could have easily adopted the step of "using an instruction sequence executed separately from an application program (application program) which uses the circuit (central processing unit 12), and determining an operation mode corresponding to the type of the application program (application program) of the circuit (central processing unit 12) " for the step of "determining an operation mode corresponding to the type of an application program (application program) of the circuit (central processing unit 12)" in the Invention.

(2) Effect of the Invention

The effect of the configuration of the Invention can be predicted by a person skilled in the art as a configuration which has been easily conceived from Cited invention, and cannot serve as grounds for approving an inventive feature of the Invention.

(3) Summary

Thus, the Invention could have been easily made by a person skilled in the art based on the Cited Invention.

6. Closing

As described above, the Invention could have easily been made by a person skilled in the art based on the Cited Invention; thus, the appellant should not be granted a patent for the Invention in accordance with the provisions of Article 29(2) of the Patent Act.

Accordingly, the present application should be rejected without examining other claims.

Therefore, the appeal decision shall be made as described in the conclusion.

September 7, 2015

Chief administrative judge: KOBIKI, Mitsuaki
Administrative judge: SHIRAISHI, Keigo
Administrative judge: YAMASAWA, Hiroshi