Appeal Decision

Appeal No. 2014-22371

Singapore
Appellant KINGLITE HOLDINGS INC.

Tokyo, Japan
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The appeal decision, which was made on September 7, 2015 regarding the case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2013-17748, entitled "Method and Apparatus for Providing Intelligent Power Management" (the application published on June 13, 2013, Japanese Unexamined Patent Application Publication No. 2013-117981), came with a court decision of revocation of the appeal decision at the Intellectual Property High Court (2016 (Gyo-Ke) No. 10023, rendition of decision on December 26, 2016); the case was proceeded further and has resulted in the following appeal decision:

Conclusion

The appeal of the case was groundless.

Reason

No. 1 History of the procedures

The present application is a divisional application filed on January 31, 2013 from Patent Application No. 2000-580071 filed on November 4, 1999 as an international filing date (priority claim under the Paris Convention, received by the foreign receiving office, November 4, 1998, the US), and a written amendment was submitted at the same time. Then, reasons for refusal were notified on October 11, 2013 and a written amendment was submitted on January 22, 2014; however, the examiner's decision of refusal was issued on June 25, 2014. Against this, an appeal against the examiner's decision of refusal was requested on November 4, 2014.

Subsequently, the appeal decision of "the appeal of the case was groundless" was made on September 7, 2015, and a certified copy of the decision was delivered to the appellant on September 29, 2015. This decision came with a court decision of revocation of the appeal decision at the Intellectual Property High Court (2016 (Gyo-Ke) No. 10023, rendition of decision on December 26, 2016) and therefore, the application was further examined, reasons for refusal (hereinafter, referred to as "the reasons for refusal by the body") were notified by the body on February 28, 2017, and an opportunity to submit a written opinion within a designated period was given. However, no response was made by the appellant.

No. 2 The Invention

The inventions relating to Claims 1-14 of the present application are acknowledged as specified by the matters described in Claims 1-14 in the scope of

claims which were amended by the written amendment dated January 22, 2014, and the inventions relating to Claims 1-3 of the present application (hereinafter, the invention relating to Claim 1 is referred to as "the Invention") are as follows:
"[Claim 1]
A power management device for a circuit in a processor-based system, comprising:
a memory to store instruction sequences which are used to process the processor-based system;
and a processor coupled to the memory; wherein
the stored instruction sequences make the processor perform the following, separately from an application program that uses the circuit:
(a) determining an operation mode corresponding to the type of the application program of the circuit; and
(b) according to the operation mode, operating the circuit at a first predetermined speed or operating the circuit at a second predetermined speed higher than the first predetermined speed."
[Claim 2]
A power management device according to Claim 1, wherein the stored instruction sequences further make the processor perform the following: (c) determining whether a predetermined activity level from an input/output device coupled to the circuit exists within a predetermine period; operating, if it exists, the circuit at a third predetermined speed; and operating, if not, the circuit at the first predetermined speed.
[Claim 3]
A power management device according to Claim 2, wherein the third predetermined speed is between the first and second predetermined speeds."

No. 3 Cited Document and Cited Invention
Japanese Unexamined Patent Application Publication No. H8-76874 (hereinafter, referred to as "Cited Document 1") that was cited in the reasons for refusal by the body includes the following descriptions A to G: The underlines have been added by the body.
A
"[0001]
[Industrial Application Field] The present invention relates to a clock control device and a clock control method of a central processing unit, and more particularly to a clock control device and a clock control method of a central processing unit which are suitable for achieving power saving of a central processing unit (hereinafter, abbreviated as "CPU") which is used in an information processing device represented by a personal computer (hereinafter, referred to as "PC") or small information terminal."
B
"[0006] Further, in recent years, a multimedia (moving images, voices, etc.) capability which requires much computation performance have been increasingly installed in a system. For example, such a case can be considered that word-processor or spreadsheet software and video conference software are operated on a single PC. Here, the former word-processor and spreadsheet software are sufficiently available if a CPU has the performance of several 10 MIPS (Million Instructions Per Second); however, the latter video conference software requires not only compression/expansion processing of moving images and voices but also a communication function, requiring

the performance of several 100 MIPS. On the other side, the CPU performance tends to rapidly become higher at an annual rate of approximately 1.6 times and can be predicted to reach the performance of several 100 MIPS in several years. However, there is an extremely large difference in power consumption between the operation states of several 10 MIPS and several 100 MIPS and therefore, it is wasteful of power consumption to make a CPU having several 100 MIPS performance operate several 10 MIPS software.

[0007] Therefore, automatically switching of the performances according to software used has been demanded; however, in the prior art, no consideration has been given to switching the CPU performances according to the operation speeds of programs.

[0008] This invention was made to solve the above problem in the prior art, and the object is to provide a clock control device and a clock control method for a CPU that can achieve operation at low power consumption even during execution of a task according to the performance of a program operated on an information processing device in a multitask operation environment in such a manner that when a processing program requiring low performance is executed, the operation clock of the CPU is automatically switched to the minimum required operation clock that satisfies its required performance, so as to save power consumption."

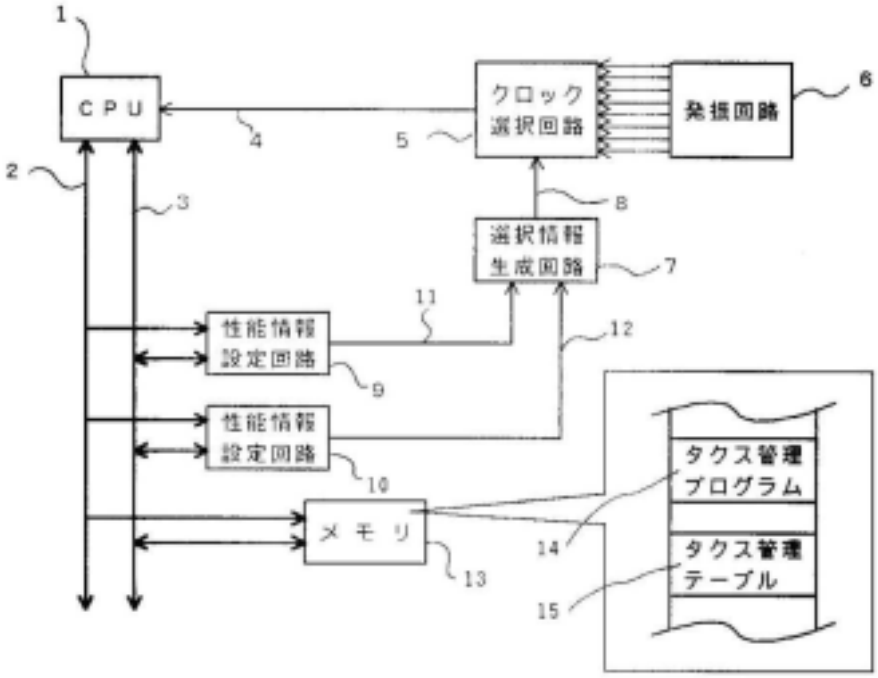
C

"[0010]

[Means for solving the problem] To achieve the above purpose, the configuration of the invention relating to the clock control device of a central processing unit in the present invention is as follows: the clock control device of a central processing unit of an information processing device, which includes a memory that stores a multitask operating system and program which are capable of starting and executing a plurality of tasks by switching them, and a central processing unit that executes the programs in the multitask operating system environment and whose operation speed is determined on the basis of a given clock frequency, is provided with: one or more performance information setting circuits that provide performance information of the central processing unit which is required for each task started in the multitask operating system environment and set the performance information of the central processing unit for each of the tasks; a selection information generation circuit that generates selection information by using one or more pieces of performance information set in the performance information setting circuit so that the clock frequency of central processing unit is determined so as to allow operation with the minimum performance required by a task in activation; an oscillation circuit that generates a plurality of clock signals; and a clock selection circuit that selects one of the plurality of clock signals according to the selection information and provides it to the central processing unit."

D

FIG. 1



性能情報設定回路　Performance information setting circuit
クロック選択回路　Clock selection circuit
選択情報生成回路　Selection information generation circuit
発振回路　Oscillation circuit
タスク管理プログラム　Task management program
タスク管理テーブル　Task management table
メモリ　Memory

E
"[0019]
[Examples] Examples according to the present invention are described below by reference to FIG. 1 to FIG. 12.
[Example 1] The first example according to the present invention is described below by reference to FIG. 1 to FIG. 6. First, the circuit configuration of the clock control device of a CPU according to the present invention will be described by reference to FIG. 1. FIG. 1 is a block diagram indicating the circuit configuration of the clock control device of a CPU according to the first example of the present invention.
[0020] In FIG. 1, an oscillation circuit 6 can generate clocks having eight types of frequencies. A selection information circuit 7 (Note by the body: the description of "selection information circuit" is considered to be an error of "selection information generation circuit"; the same shall apply hereinafter) is a circuit to control a clock selection circuit 5. Performance information setting circuits 9 and 10 are circuits for holding load information of tasks. In a memory 13, programs and data used by the CPU 1 are stored. In addition, as shown in the figure, a task management program 14 and a task management table 15 are stored in the memory 13.

[0021] For the CPU 1, eight operation level states can be specified at intervals of MIPS from 5 to 40 MIPS. The oscillation circuit 6 outputs clocks having eight types of frequencies corresponding to the above levels.
[0022] In addition, the information processing device according to the present invention is based on the premise of having a multitask OS (operating system) starting and executing various programs on the OS. The OS includes a task management program 14 for controlling the starting and ending of a task. In addition, various kinds of information required for controlling the task management program 14 are included in the task management table 15. More specifically, in addition to a task ID for uniquely identifying each task, a memory capacity required, etc., performance information and a pending flag which are characteristic of the present invention exist as items to be registered for each task.
[0023] The performance information represents the capacity of a CPU load specified according to the content of a program executed by each task. The pending flag is a flag indicating a wait state for setting performance information of a task in the performance information setting circuit.
[0024] The role of the pending flag will become clear when the operation of the present invention is described using a flow later; therefore, the performance information is described first. The performance information is specified according to the content of a program executed by a task, as described above. For example, as for programs of a word processor, it is assumed that an edit program requires the CPU performance of 10 MIPS and a print program requires the CPU performance of 5 MIPS.
[0025] In such a situation, when the task management program 14 sets performance information of 10 MIPS to the performance information setting circuit 9 in starting a task of the edit program, the selection information circuit 7 generates selection information corresponding to the operation frequency of the CPU 1 equivalent to 10 MIPS. According to this selection information, the clock selection circuit 5 selects a relevant clock and supplies it to the CPU 1 via a clock line 4. Thus, the CPU 1 operates at 10 MIPS. The above is a basic mechanism of the present invention.
[0026] Then, in printing a document edited by the word processor, the task management program 14 starts a task of the print program. At this time, it sets performance information of 5 MIPS to the performance information setting circuit 10. The selection information circuit 7 generates selection information corresponding to the operation frequency of the CPU 1 equivalent to 15 MIPS, from the performance information of 10 MIPS which is set in the performance information setting circuit 9 and the performance information which is set in the performance information setting circuit 10. According to this selection information, the clock selection circuit 5 selects a relevant clock and supplies it to the CPU 1 via the clock line 4. Thus, the CPU 1 transitions from 10 MIPS to 15 MIPS, a higher-speed operation mode.
[0027] The performance information is represented by a processing capability per unit time and therefore, it should be noted that when two tasks are executed in parallel, the performance information shows the sum of the two tasks.
[0028] According to the present invention, as described above, even when printing is executed during editing on a word processor, the performance of the CPU 1 can be improved so as to match a load thereof and a sufficient operation environment for editing even during printing can be obtained."
F

"[0074] [Example 3] The third example according to the present invention is described below by reference to FIG. 8 to FIG. 10. FIG. 8 is a block diagram indicating the circuit configuration of the clock control device of a CPU according to the third example of the present invention.
[0075] The feature of the third example is that a selection information setting circuit 70 generates selection information, which is generated by the performance information setting circuits 9 and 10 and the selection information setting circuit 7 in the first example, according to a task management program 71 shown in FIG. 8.
[0076] In this case, the selection information setting circuit 70 is a circuit for setting selection information provided to the clock selection circuit 5, and the task management program 71 is a program having a function to generate selection information.
[0077] The function of this selection information setting circuit 70 will be described in detail below by reference to FIG. 9. FIG. 9 is a block diagram indicating the circuit configuration of the selection information setting circuit according to the third example of the present invention.
[0078] Also in this example, the available performance level is assumed to be at eight level steps and therefore, the register 80 consists of 3 bits. In the selection information setting circuit 70, the CPU 1 can set the performance information of 3 bits and read the set performance information via the address bus 2 and the data bus 3. Unlike Example 1, the performance information to be set is not generated by the performance information setting circuit but is generated by the task management program 71. This performance information is transmitted to the decoder circuit 35 in the selection information setting circuit 70, and the decoder circuit 35 generates clock selection information from the above performance information and outputs it to the selection information signal line 8, thereby causing the operation frequency of the CPU 1 to be determined in the end."
G
"[0087] As described above, by providing the task management program 71 with a function for generating selection information given to the CPU 1 from the performance information at the time of starting and ending a task, this function can be implemented by software. Therefore, this example, unlike Example 1, does not require the performance information setting circuits 9 and 10, and has the advantage of allowing reduction in the number of hardware parts."

a.

Here, according to the descriptions of paragraphs [0001], [0008], and [0010], the Cited Document 1 describes:
"a clock control device of a CPU which achieves power saving of the CPU used in an information processing device and is provided with:
one or more performance information setting circuits that provide performance information of the CPU which is required for each started task and set the performance information of the CPU for the each task; a selection information generation circuit that generates selection information for determining a clock frequency of the CPU so as to allow operation with the minimum performance required by a task in activation by using one or more pieces of performance information set in the performance information setting circuit; an oscillation circuit that generates a plurality of clock signals; and a clock selection circuit that selects one of the plurality of clock signals

according to the selection information and provides it to the CPU."

b.

According to the descriptions of paragraphs [0019] and [0020], the "clock control device of a CPU" of the above a. has a memory, in which a task management program is stored together with the programs and data used by the CPU.

Accordingly, the "clock control device of a CPU" of the above a. includes "a memory in which a task management program is stored together with the programs used by the CPU."

c.

According to the description of paragraph [0022], the "information processing device" of the above a. is for "executing various programs on the OS" and the "task management program" in the above b. is included in the OS and "controls the starting and ending of a task." In addition, since it is obvious that the programs and OS are executed on the CPU in the information processing device, the "CPU" in the above a. "executes various programs on the OS which includes a task management program for controlling the starting and ending of a task."

d.

According to the description of paragraph [0023], to "provide performance information of the CPU which is required for each started task" in the above a. is to "provide the performance information representing the capacity of a CPU load specified according to the content of a program executed by each task."

e.

According to the descriptions of paragraphs [0024] to [0026], the "task management program" sets, in starting a task of a program, performance information according to the content of the program executed by the task, in two performance information setting circuits; and the selection information generation circuit generates selection information on the basis of the setting information of the two performance information setting circuits.

f.

According to the descriptions of paragraphs [0020] and [0021], it is described as a specific example that "For the CPU, eight operation levels states can be specified at intervals of MIPS from 5 to 40 MIPS. The oscillation circuit outputs clocks having eight types of frequencies corresponding to the above levels."

g.

According to the descriptions of paragraphs [0024] to [0026], it is described as a specific example that:

"as for programs of a word processor, an edit program requires the CPU performance of 10 MIPS and a print program requires the CPU performance of 5 MIPS; the task management program sets performance information of 10 MIPS to the performance information setting circuit 9 in starting a task of the edit program; then, the selection information generation circuit generates selection information corresponding to the operation frequency of the CPU 1 equivalent to 10 MIPS; according to this selection information, the clock selection circuit selects a relevant clock and supplies the clock for operation at 10 MIPS to the CPU; further, the task management program sets the performance information of 5 MIPS to the performance information setting circuit 10 in starting a task of the print program, then, the selection information generation circuit generates selection information corresponding to the operation frequency of the CPU

equivalent to 15 MIPS from the performance information of 10 MIPS set in the performance information setting circuit 9 and the performance information of 5 MIPS set in the performance information setting circuit 10; and according to the selection information, the clock selection circuit selects a relevant clock and supplies the clock for operation at 15 MIPS to the CPU."

h.

Therefore, according to the above a. to g., the following invention (hereinafter, referred to as "Cited Invention") is described in Cited Document 1:

"A clock control device of a CPU which achieves power saving of the CPU used in an information processing device, comprising:

a memory in which a task management program is stored together with programs used by the CPU; wherein

the CPU executes various programs on an OS which includes the task management program for controlling the starting and ending of a task;

performance information representing the capacity of a CPU load specified according to the content of a program executed by each task is provided;

the task management program sets, in starting a task of a program, performance information according to the content of the program executed by the task, in two performance information setting circuits; and

the selection information generation circuit includes: a selection information generation circuit that generates selection information for determining the clock frequency of the CPU so as to allow operation with the minimum performance required by a task in activation, on the basis of the setting information of the two performance information setting circuits;

an oscillation circuit that generates a plurality of clock signals; and a clock selection circuit that selects one of the plurality of clock signals and provides it to the CPU; and further wherein

as a specific example,

for the CPU, eight operation level states can be specified at intervals of MIPS from 5 to 40 MIPS and the oscillation circuit outputs clocks having eight types of frequencies corresponding to the above levels;

as for programs of a word processor, an edit program requires the CPU performance of 10 MIPS and a print program requires the CPU performance of 5 MIPS;

when the task management program sets performance information of 10 MIPS to the performance information setting circuit 9 in starting a task of the edit program, the selection information generation circuit generates selection information corresponding to the operation frequency of the CPU 1 equivalent to 10 MIPS, and according to this selection information, the clock selection circuit selects a relevant clock and supplies the clock for operation at 10 MIPS to the CPU; and

further, when the task management program sets performance information of 5 MIPS to the performance information setting circuit 10 in starting a task of the print program, the selection information generation circuit generates selection information corresponding to the operation frequency of the CPU equivalent to 15 MIPS from the performance information of 10 MIPS set in the performance information setting circuit 9 and the setting information of 5 MIPS set in the performance information setting circuit 10, and according to this selection information, the clock selection circuit selects a relevant clock and supplies the clock for operation at 15 MIPS to the CPU."

No. 4 Judgment by the body
1 Regarding Article 29(2) of the Patent Act (inventive step)
A Comparison
The Invention and the Cited Invention are compared.
a.
The "information processing device" of the Cited Invention includes a "CPU," and "CPU" is an abbreviation of "Central Processing Unit" and is obviously a "processor," and therefore, the "information processing device" of the Cited Invention corresponds to the "processor-based system" of the Invention.
In addition, the "CPU" of the Cited Invention is obviously a "circuit" of the "information processing device" and therefore, the "CPU" of the Cited Invention can be said to be the "circuit of the processor-based system" of the Invention.
Further, the Cited Invention is "a clock control device of a CPU which achieves power saving" and achieves power saving by changing the operation clock frequency of the CPU and therefore, it can be said that "power management" is performed.
Accordingly, the "clock control device of a CPU which achieves power saving of the CPU used in an information processing device" in the Cited Invention can be said to be a "power management device for a circuit in a processor-based system" similar to the Invention.
b.
It is obvious that the "task management program" of the Cited Invention includes a plurality of instructions and is used for processing in an information processing device and therefore, the "memory in which a task management program is stored together with the programs used by the CPU" of the Cited Invention corresponds to the "memory to store instruction sequences which are used to process the processor-based system" of the Invention.
c.
In the Cited Invention, it is obvious that the CPU reads various programs and a task management program from a memory and executes them; and in FIG. 1, the CPU is coupled to the memory. Therefore, the "CPU" of the Cited Invention is a "processor coupled to the memory" similar to the Invention.
d.
It is obvious that the "task management program" of the Cited Invention is a program different from various programs such as a word processor, an edit program of the word processor, and a print program of the word processor; and the programs of the word processor are application programs. Therefore, the "task management program" of the Cited Invention operates the processor in a manner similar to the Invention in which "the stored instruction sequences make the processor perform ..., separately from an application program that uses the circuit."
e.
The "performance information" of the Cited Invention represents "the capacity of a CPU load specified according to the content of a program executed by each task," and as a specific example, it "specifies eight operation level states ... at intervals of MIPS from 5 to 40 MIPS" and "as for programs of a word processor, an edit program requires the CPU performance of 10 MIPS and a print program requires the CPU performance of 5 MIPS." In addition, the "performance information" is for determining the operation

clock frequency of the CPU and therefore, the "performance information" in the Cited Invention is for determining the "operation mode of the circuit."

Then, the feature of "the task management program sets, in starting a task of a program, performance information according to the content of the program executed by the task, in two performance information setting circuits" in the Cited Invention and the feature of "(a) determining an operation mode corresponding to the type of the application program of the circuit" in the Invention are common in the point of "(a) determining an operation mode corresponding to a program of the circuit."

f.

In the Cited Invention, "when the task management program sets performance information of 10 MIPS to the performance information setting circuit 9, the selection information generation circuit generates selection information corresponding to the operation frequency of the CPU 1 equivalent to 10 MIPS, and according to this selection information, the clock selection circuit selects a relevant clock and supplies the clock for operation at 10 MIPS to the CPU" and therefore, it can be said to supply a clock for operation at 10 MIPS to the CPU according to the "setting information" (operation mode) of "10 MIPS"; that is, "to operate the circuit at a first predetermined speed."

In addition, in the Cited Invention, "when the task management program sets performance information of 5 MIPS to the performance information setting circuit 10 in starting a task of the print program, the selection information generation circuit generates selection information corresponding to the operation frequency of the CPU equivalent to 15 MIPS from the performance information of 10 MIPS set in the performance information setting circuit 9 and the setting information of 5 MIPS set in the performance information setting circuit 10, and according to this selection information, the clock selection circuit selects a relevant clock and supplies the clock for operation at 15 MIPS to the CPU"; and therefore, it can be said to supply a clock for operation at 15 MIPS according to the "setting information" (operation modes) of "10 MIPS" and "5 MIPS"; that is, "operating the circuit at a second predetermined speed higher than the first predetermined speed."

B Corresponding features and different feature

According to the above A, there are the following corresponding features and different feature between the Invention and Cited Invention.

[Corresponding features]

"A power management device for a circuit in a processor-based system, comprising:

a memory to store instruction sequences which are used to process the processor-based system; and

a processor coupled to the memory; wherein

the stored instruction sequences make the processor perform the following, separately from an application program that uses the circuit:

(a) determining an operation mode corresponding to the program of the circuit;

(b) according to the operation mode, operating the circuit at a first predetermined speed or operating the circuit at a second predetermined speed higher than the first predetermined speed."

[Different feature]

In the Invention, the operation mode is determined according to "the type of an application program"; whereas, in the Cited Invention, the operation mode is determined according to a "program" and there is neither specification of "application program" nor specification of "type."

C Examination on the different feature

The [Different feature] in the above B will be examined below.

In the specific example in the Cited Invention 1, performance information is set for "an edit program of the word processor" and "a print program of the word processor"; performance information is set for individual programs constituting the application program of a word processor.

However, paragraph [0006] of Cited Document 1 describes that the "word-processor and spreadsheet software" require a CPU having "the performance of several 10 MIPS" and "video conference software" requires "the performance of several 100 MIPS"; and paragraph [0007] describes that "automatical switching of the performances according to software used was demanded." Therefore, a person skilled in the art could have easily conceived of broadly setting the performance information of several 10 MIPS for the application program of a word processor, not for individual programs of a word processor.

In addition, the "performance information" of the Cited Invention represents "the capacity of a CPU load specified according to the content of a program executed by each task," and as a specific example, it specifies "eight operation level states ... at intervals of MIPS from 5 to 40 MIPS;" therefore, one of eight levels is specified as performance information for a program executed as a task. Then, even when performance information is set for an application program as described above, it is commonly considered that any plurality of programs in programs are at an identical level, and it can be said that a plurality of programs at an identical level is of an identical "program type."

As for the "program type" in the present application, the demandant, who is a plaintiff in the prior case regarding the present application (2016 (Gyo-Ke) No. 10023, a request to revoke the appeal decision), alleges on page 2 in the second brief which was submitted on June 6, 2016 that: "'type' is a generally used word and it obviously means '(type) (1) category, format, or a category classified in terms of having a certain similarity for a plurality of goods, people and things' (note by the body: number 1 enclosed by a circle in the original text is shown as (1).) (page 3, lines 3 to 5 on the first brief of the plaintiff); and therefore, it does not make the invention according to the claims unclear even without description thereof in the specification. In the specification, word processing, a presentation service, and a spreadsheet service are illustrated as application programs. In the Invention, these application programs are classified; for example, the word processing and presentation service are classified into one group and one (identical) operation mode is determined for the group, and the spreadsheet service is classified into another group and another operation mode is determined for the group (paragraphs [0025] and [0026] of Evidence A No.3 (note by the body: 'Evidence A No.3' is publication before examination of the present application, Japanese Unexamined Patent Application Publication No. 2013-117981.)). Application programs are classified by using read profile IDs and corresponding operation modes are determined; and therefore, groups of classified programs can be

said to be 'types of application programs.' In addition, the specification describes processing for determining an operation mode and setting a device clock according to the operation mode; and therefore, it describes information processing according to the 'types of application programs.'"

Thus, a person skilled in the art could have easily conceived of making the "operation mode" correspond to a "program type" in the Cited Invention.

D Summary

As described above, the Invention could have easily been made by a person skilled in the art based on the Cited Invention; thus, the appellant should not be granted a patent for the Invention in accordance with the provisions of Article 29(2) of the Patent Act.

2 Regarding Article 17-2(3) of the Patent Act (new matter)

Amendment made by the written amendment dated January 22, 2014 and amendment made by the written amendment dated January 31, 2013 are amendment including the amended matter of "the third predetermined speed is between the first and second predetermined speeds" for Claim 3.

The specification, scope of claims, or drawings of the translation of the foreign language document of the present application (hereinafter, referred to as "the translation and the like.") include the following description:

"[Claim 14]

A device according to Clam 13, wherein the stored instruction sequences further make the processor perform the following: (c) determining whether a predetermined activity level from an input/output device coupled to the circuit exists within a predetermined period; operating, if it exists, the circuit at the second predetermined level on the basis of the activity level; and operating, if not, the circuit at the third predetermined level."

"[Claim 28]

A method according to Claim 27, further including (c) determining whether a predetermined activity level from an input/output device coupled to the circuit exists within a predetermined period; operating, if it exists, the circuit at the second predetermined level on the basis of the activity level; and operating, if not, the circuit at the third predetermined level."

"[Claim 42]

A computer-readable device according to Claim 41, wherein the stored instruction sequences further make the processor perform the following: (c) determining whether a predetermined activity level from an input/output device coupled to the circuit exists within a predetermine period; operating, if it exists, the circuit at the second predetermined level on the basis of the activity level; and operating, if not, the circuit at the third predetermined level."

"[0027]

In the determination block 408, when the process 400 determines that the profile ID does not indicate that the device provides a spreadsheet service, it proceeds to the determination block 412 and determines whether there is any action from an I/O device such as a keyboard, mouse, or disk drive within a predetermined period. In one embodiment, the predetermined period is one minute. When there is no action, the

process 400 proceeds to the process block 414 and sets the device clock to the minimum. The process returns to the flow of the main process. In the determination block 412, when the process 400 determines that there is an action from an I/O device within the predetermined period, the process 400 proceeds to the process block 416 and sets the device clock to device_clock=D*device_clock, where D is a predetermined number. Then, the process 400 returns to the flow of the main process 100."

Thus, the translation and the like only describe that when there is no action, the device clock is set to the minimum and when there is any action, the device clock is set "to device_clock=D*device_clock," and "D is a predetermined number;" and they describe neither the meaning of the "device_clock" on the right side of "device_clock=D*device_clock" nor a specific example of the number D.

Accordingly, the translation and the like do not describe a relative high/low relation between "the third predetermined speed" which is a clock for the case where it is determined that there is any action and the first predetermined speed/second predetermined speed; and therefore, the amended matter of "the third predetermined speed is between the first and second predetermined speeds" is neither a matter that is described in the translation and the like nor a matter that is obvious from matters described in the translation and the like.

Therefore, amendment made by the written amendment dated January 22, 2014 and amendment made by the written amendment dated January 31, 2013 were not made within the scope of the matters described in the translation and the like of the foreign language document and thus do not meet the requirement stipulated in Article 17-2(3) of the Patent Act.

3. Regarding Article 36(6)(i) of the Patent Act (requirements for support)

As to the description of "the third predetermined speed is between the first and second predetermined speeds" in Claim 3 of the present application,
paragraph [0027] of the specification describes that "In the determination block 408, when the process 400 determines that the profile ID does not indicate that the device provides a spreadsheet service, it proceeds to the determination block 412 and determines whether there is any action from an I/O device such as a keyboard, mouse, or disk drive within a predetermined period. In one embodiment, the predetermined period is one minute. When there is no action, the process 400 proceeds to the process block 414 and sets the device clock to the minimum. The process returns to the flow of the main process. In the determination block 412, when the process 400 determines that there is an action from an I/O device within the predetermined period, the process 400 proceeds to the process block 416 and sets the device clock to device_clock=D*device_clock, where D is a predetermined number. Then, the process 400 returns to the flow of the main process 100."

Then, the detailed description of the invention in the specification describes that when there is no action, the device clock is set to the minimum and when there is any action, the device clock is set "to device_clock=D*device_clock," and "D is a predetermined number"; however, the specification does not make it clear what "device_clock" on the right side of "device_clock=D*device_clock" means, and does not describe a specific example of the number, D. Therefore, the feature that "the third predetermined speed" which is a clock for the case where it is determined that there is any action "is between the first and second predetermined speeds" is not described in

the detailed description of the invention.

Therefore, the invention according to Claim 3 of the present application is not described in the detailed description of the invention and thus, does not meet the requirement stipulated in Article 36(6)(i) of the Patent Act.

No. 5 Closing

As described above, the Invention could have easily been made by a person skilled in the art based on the Cited Invention; thus, the appellant should not be granted a patent for the Invention in accordance with the provisions of Article 29(2) of the Patent Act.

In addition, amendment made by the written amendment dated January 22, 2014 and amendment made by the written amendment dated January 31, 2013 were not made within the scope of the matters described in the translation and the like of the foreign language document and thus do not meet the requirement stipulated in Article 17-2(3) of the Patent Act.

Further, the invention according to Claim 3 of the present application is not described in the detailed description of the invention and thus, does not meet the requirement stipulated in Article 36(6)(i) of the Patent Act.

Thus, the present application should be rejected without examining other claims.

Therefore, the appeal decision shall be made as described in the conclusion.

August 7, 2017

Chief administrative judge: SHINKAWA, Keiji
Administrative judge: TAKASE, Tsutomu
Administrative judge: YAMADA, Masafumi