Appeal decision

Appeal No. 2015-12454

Korea
Appellant SAMSUNG ELECTORONICS CO. LTD.

Tokyo, Japan
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The case of appeal against an examiner's decision of refusal of Japanese Patent Application No. 2010-280545, "Flash memory device and reading-out method thereof" [the application published on Aug. 25, 2011: Japanese Unexamined Patent Application Publication No. 2011-165301] has resulted in the following appeal decision:

Conclusion

The appeal of the case was groundless.

Reason

No. 1 History of the procedures

The present application is an application filed on Dec. 16, 2010 (Priority Claim under the Paris Convention: Feb. 8, 2010 (hereinafter, referred to as "Priority date"), Republic of Korea), and although, against a notice of reasons for refusal dated Jun. 13, 2014, an opinion and amendment were made on Sep. 12 of the same year, a decision of refusal was made on Feb. 27, 2015(dispatch of a copy of the original on Mar. 3 of the same year). In response to this, a demand for appeal against the examiner's decision of refusal was made on Jul. 1 of the same year, and, in conjunction with this, an amendment was made, followed by issuance of a report prescribed in Article 164(3) of the Patent Act (a reconsideration report made to the JPO Commissioner in the procedure of reconsideration by examiners before appeal proceedings) dated Jul. 31 in the same year.

No. 2 Decision to dismiss amendment for the Amendment dated Jul. 1, 2015

[Conclusion of Decision to Dismiss Amendment]

The amendment dated Jul. 1, 2015 (hereinafter, referred to as "The Amendment

") shall be dismissed.

[Reason]
1 Details of Amendment
(1) The statements of Claims after the Amendment
The amendment dated Jul. 1, 2015 is an amendment to amend the statements of the scope of claims amended by the Amendment dated Sep. 12, 2014 of

"[Claim 1]
A flash memory device comprising:
a memory cell array including a plurality of memory cells;
a control logic configured to control a read operation on the memory cells;
a page buffer circuit configured to sense hard decision data and a plurality of soft decision data from each of a plurality of selected memory cells in response to the control of the control logic and output the sensed hard decision data and the plurality of soft decision data as a read result; and
a voltage generation circuit configured to generate a plurality of read voltages for reading the hard decision data and the plurality of soft decision data in response to the control of the control logic, wherein
the plurality of soft decision data are sensed between adjacent pieces of threshold voltage distribution.
[Claim 2]
The flash memory device of claim 1, wherein the voltage generation circuit generates a reference voltage for reading the hard decision data and a plurality of variable read voltages for reading the plurality of soft decision data.
[Claim 3]
The flash memory device of claim 1, wherein the plurality of soft decision data included in the read result are outputted in the format sensed by the page buffer circuit, or are encoded and outputted as reliability data.
[Claim 4]
The flash memory device of claim 3, wherein the reliability data are internally encoded in the page buffer.
[Claim 5]
The flash memory device of claim 3, wherein the read result includes the hard decision data of 1 bit and the reliability data of i bits (where i is a positive integer).
[Claim 6]

The flash memory device of claim 3, wherein

the page buffer circuit includes a plurality of page buffers corresponding respectively to the selected memory cells, and each of the page buffers includes a plurality of first type latches configured to encode the reliability data by a latched value toggled in response to a value of the plurality of soft decision data and a second type latch configured to latch the hard decision data.

[Claim 7]

The flash memory device of claim 1, wherein the read result includes the hard decision data of 1 bit and the plurality of soft decision data of j bits (where j is a positive integer).

[Claim 8]

A read method of a flash memory device, comprising:

generating a reference voltage for reading hard decision data from each of selected memory cells and a plurality of variable read voltages;

sensing the hard decision data and a plurality of soft decision data by applying the reference voltage and the plurality of variable read voltages to the selected memory cells; and

outputting the sensed hard decision data and the plurality of soft decision data as a read result, wherein

the plurality of soft decision data are sensed between adjacent pieces of threshold voltage distribution and outputted in the sensed format, or are encoded and outputted as reliability data.

[Claim 9]

The read method of claim 8, wherein the reliability data are internally encoded in the page buffer.

[Claim 10]

The read method of claim 8, wherein the reliability data are encoded by the latched values of at least two latches of page buffers corresponding respectively to the selected memory cells being toggled in response to the values of the plurality of soft decision data corresponding respectively to the selected memory cells." (hereinafter, the claims described in this scope of claims are referred to as "Claims before Amendment") to

"[Claim 1]

A flash memory device comprising:

a memory cell array including a plurality of memory cells;

a control logic configured to control a read operation on the memory cells;

a page buffer circuit configured to sense hard decision data and a plurality of soft decision data from each of a plurality of selected memory cells in response to the control of the control logic and output the sensed hard decision data and the plurality of soft decision data as a read result; and

a voltage generation circuit configured to generate a plurality of read voltages for reading the hard decision data and the plurality of soft decision data in response to the control of the control logic, wherein

the plurality of soft decision data are sensed between adjacent pieces of threshold voltage distribution, wherein

the plurality of soft decision data included in the read result are encoded into reliability data to be outputted, wherein

the page buffer circuit includes a plurality of page buffers corresponding respectively to the selected memory cells, wherein

each of the page buffers includes a plurality of first type latches to encode the reliability data by values latched in response to values of the plurality of soft decision data being toggled and a second type latch to latch the hard decision data, and wherein

the reliability data are expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data by being encoded in the plurality of first type latches.

[Claim 2]

The flash memory device of claim 1, wherein the voltage generation circuit generates a reference voltage for reading the hard decision data and a plurality of variable read voltages for reading the plurality of soft decision data.

[Claim 3]

The flash memory device of claim 1, wherein the reliability data are internally encoded in the page buffer.

[Claim 4]

The flash memory device of claim 1, wherein the read result includes the hard decision data of 1 bit and the reliability data of i bits (where i is a positive integer).

[Claim 5]

A read method of a flash memory device, comprising:

generating a reference voltage for reading hard decision data from each of selected memory cells and a plurality of variable read voltages;

sensing the hard decision data and a plurality of soft decision data by applying the reference voltage and the plurality of variable read voltages to the selected memory cells; and

outputting the sensed hard decision data and the plurality of soft decision data as a read result, wherein

the plurality of soft decision data are sensed between adjacent pieces of threshold voltage distribution, and encoded into reliability data to be outputted, wherein

the reliability data are encoded by the latched values of at least two latches of page buffers corresponding respectively to the selected memory cells being toggled in response to the values of the plurality of soft decision data corresponding respectively to the selected memory cells, and wherein

the reliability data are expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data by being encoded in the at least two latches.

[Claim 6]

The read method of claim 5, wherein the reliability data are internally encoded in the page buffer." (Hereinafter, the claims described in this scope of claims are referred to as "Claims after Amendment").

(2) The Amended matters

When Claims before Amendment and Claims after Amendment are compared with each other, it is obvious that claims 1, 3, and 6 before amendment were amended as claim 1 after amendment, claims 8 and 10 before amendment were amended as claim 5 after amendment, claims 4, 5, and 9 before amendment were amended in only their claim numbers, and claims 2, 4, 5, and 9 before amendment correspond to claims 2, 3, 4, and 6 after amendment.

Accordingly, the Amendment consists of the following amended matters 1 to 5.

<Amended matter 1>

An amendment that, regarding "soft decision data" of claim 1 before amendment, a limitation matter of "the plurality of soft decision data included in the read result are encoded into reliability data to be outputted" is added to make it claim 1 after amendment.

<Amended matter 2>

An amendment that, regarding "page buffer circuit" of claim 1 before amendment, a limitation matter of "the page buffer circuit includes a plurality of page buffers corresponding respectively to the selected memory cells, wherein each of the page buffers includes a plurality of first type latches to encode the reliability data by

values latched in response to values of the plurality of soft decision data being toggled and a second type latch to latch the hard decision data" is added to make claim 1 after amendment.

<Amended matter 3>

An amendment that, about "reliability data" of claim 1 before amendment, a limitation matter of "the reliability data are expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data by being encoded in the plurality of first type latches" is added to make claim 1 after amendment.

<Amended matter 4>

An amendment that, about "reliability data" of claim 8 before amendment, a limitation matter of "the reliability data are encoded by the latched values of at least two latches of page buffers corresponding respectively to the selected memory cells being toggled in response to the values of the plurality of soft decision data corresponding respectively to the selected memory cells" is added to make claim 5 after amendment.

<Amended matter 5>

An amendment that, about "reliability data" of claim 8 before amendment, a limitation matter of "the reliability data are expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data by being encoded in the at least two latches" is added to make claim 5 after amendment.

2 New matters and the requirement for technical feature change (shift amendment)

Whether the Amendment has been made within the matters described in the description, the scope of claims, or drawings originally attached to the application; that is, whether or not it complies with the prescriptions of Article 17-2(3) of the Patent Act, and whether it is not one that tries to change a special technical feature (shift amendment); that is, whether or not it complies with the prescriptions of Article 17-2(4) of the Patent Act, will be examined below.

(1) The Amended matter 1 is one that has been made based on the matters described in claim 3 before amendment.
(2) The Amended matter 2 is one that has been made based on the matters described in claim 6 before amendment.
(3) Regarding the Amended matters 3 and 5, although direct statements cannot be

confirmed from the matters described in the description, the scope of claims, or drawings originally affixed to the application, when the allegation that "the Amendment of (g) is based on the statements of paragraphs [0049]-[0060] of the description and Figure 8" in the above-mentioned demand for appeal against an examiner's decision of refusal dated Jul. 1, 2015 is taken into consideration, there is described in the description of the present application ([0049]) that "although a data format sensed in the seven-times of repeated read operations is identical with that of FIG. 7, data outputted actually have a predetermined data pattern as shown in FIG. 8. (Omitted) Read data outputted through the page buffer PB can be constituted by 1 bit of hard decision data and 2 bits of reliability data.", and, therefore, it can be understood as there is described that a data format sensed in the seven times of repeated read operations is constituted into one bit of hard decision data and two bits of reliability data. In addition, since read results sensed from memory cells belonging to each zone of the pieces of distribution of threshold voltages are latched as values of soft decision data (6 bits) and hard decision data (1 bit), toggling or sustaining a state just as it is repeated, and are expressed (encoded) as reliability data (2 bits) and hard decision data (1 bit), it can be understood that reliability data are of a number of bits (2 bits) less than the number of bits necessary for expressing decision data (7 bits), and, therefore, it is recognized that there is described in paragraphs [0050] to [0060] an aspect of the limitation matter to be added to "reliability data". Furthermore, it is also obvious that the amendment is not one to try to change a special technical feature (shift amendment).

(4) The Amended matter 4 is an amendment that has been made based on the matters described in claim 10 before amendment.

(5) From the above, the Amendment has been made within the matters described in the description, the scope of claims, or the drawings originally affixed to the application, and complies with the prescriptions of Article 17-2(3) of the Patent Act.

In addition, the Amendment is not one that tries to change a special technical feature (shift amendment), and it complies with the prescriptions of the Patent Act Article 17-2(4).

3 Purpose requirements

Since the Amendment is an amendment that was made at the same time as the above-mentioned demand for appeal against an examiner's decision of refusal dated Jul. 1, 2015, and aims at amending the scope of claims, it will be examined below whether or not the Amendment satisfies the prescriptions of Article 17-2(5) of the Patent Act; that is, whether or not the Amendment is one that aims at any of: deletion of claims

specified in Article 17-2(5) of the Patent Act; restriction of the scope of claims (limited to the cases where the restriction is to restrict matters required to identify the invention stated in a claim or claims under Article 36(5) of the Patent Act, and the industrial applicability and the problem to be solved of the invention stated in said claim or claims prior to the Amendment are identical with those after the Amendment); the correction of errors; and the clarification of an ambiguous description (limited to the matters stated in the reasons for refusal in the notice of reasons for refusal).

(1) Amended matters 1 to 5

The Amended matters 1 to 5 are amendments for the purpose of limitation of matters specifying the invention of claims 1 and 8 before amendment, and thus it is obvious that even by the Amendment, the field of industrial application and problems to be solved of the inventions according to claims before Amendment and those of the inventions described in claims after Amendment are identical.

Therefore, the above-mentioned Amended matters 1 to 5 are for the purpose of restriction in a limited way, and thus it can be said that the Amendment falls under the category of ones for the purpose of the deletion of claims prescribed in Article 17-2(5)(i) of the Patent Act and restriction of the scope of claims prescribed in Article 17-2(5)(ii) of the Patent Act. Accordingly, it complies with the provisions of Article 17-2(5) of the Patent Act.

4 Judgment on independent requirements for patentability

The amendment is one that includes the above-mentioned Amended matters 1 to 5 for the purpose of restricting the scope of claims (restriction in a limited way) prescribed in Article 17-2(5)(ii) of the Patent Act. Therefore, whether or not the invention according to claim 1 after amendment made by amendment aiming at the restriction in a limited way (hereinafter, referred to as "the Amended Invention") is one for which the appellant can be granted a patent independently at the time of its filing (whether it complies with the provisions of Article 126(7) of the Patent Act as applied mutatis mutandis pursuant to the provisions of Article 17-2(6) of the same Act) will be examined below.

(1) The Amended Invention

It is recognized that, seen from the statements of the scope of claims, the description, and the drawings amended by the above-mentioned amendment dated Jul. 1, 2015, the Amended Invention is as follows according to claim 1 of the scope of claims.

"A flash memory device comprising:

a memory cell array including a plurality of memory cells;

a control logic configured to control a read operation on the plurality of memory cells;

a page buffer circuit configured to sense hard decision data and a plurality of soft decision data from each of a plurality of selected memory cells in response to the control of the control logic and output the sensed hard decision data and the plurality of soft decision data as a read result; and

a voltage generation circuit configured to generate a plurality of read voltages for reading the hard decision data and the plurality of soft decision data in response to the control of the control logic, wherein

the plurality of soft decision data are sensed between adjacent pieces of threshold voltage distribution, wherein

the plurality of soft decision data included in the read result are encoded into reliability data to be outputted, wherein

the page buffer circuit includes a plurality of page buffers corresponding respectively to the selected memory cells, wherein

each of the page buffers includes a plurality of first type latches to encode the reliability data by values latched in response to values of the plurality of soft decision data being toggled and a second type latch to latch the hard decision data, and wherein

the reliability data are expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data by being encoded in the plurality of first type latches."

(2) Cited Document

(2-1) Technical matters described in Cited Document

In Japanese Unexamined Patent Application Publication No. 2008-16092 (the application published on Jan. 24, 2008, and hereinafter, referred to as "Cited Document 1") that was distributed in advance of the Priority date of the present application, and that was cited in the notice of reasons for refusal dated Jun. 13, 2014 that is the reason of the decision of refusal of the original examination, there are described the following technical matters.

(Note for the body: Underlines were added by the body for reference)

A "[0001]

The present invention relates to a nonvolatile semiconductor storage system, and, more particularly, to a nonvolatile semiconductor storage system including a nonvolatile semiconductor device capable of storing two or more bits of data (multi-bit data) in one memory cell.

(Omitted)

[0021]

[Memory configuration]

FIG. 4 illustrates a configuration of a system including a NAND cell flash memory to store four values (2 bits) as an example of a nonvolatile semiconductor storage system. This flash memory includes a memory cell array 1 configured by arranging memory cells to store data in matrix. The memory cell array 1 includes a plurality of bit lines, a plurality of word lines and a common source line, and electrically data-rewritable memory cells are arranged in matrix at intersection points of the bit lines and the word lines. In a memory cell, in addition to multi-valued data as information bits, there can be stored redundant data added to the information bits for error correction, and the above described flag data FLAG.

[0022]

In this memory cell array 1, a bit control circuit 2 for controlling bit lines, and a word line control circuit 6 for controlling word line voltages are connected. In other words, the bit line control circuit 2 is a sense amplifier and data latch circuit that has a data latch function to hold read data and write data in addition to a function to read data of memory cells in the memory cell array 1 through a bit line. In addition, the bit line control circuit 2 performs writing to memory cells in the memory cell array 1 by applying write control voltage to the memory cells through a bit line.

[0023]

To the bit line control circuit 2, a column decoder 3, a data input-output buffer 4 and a data input-output terminal 5, and a controller 11 are connected.

Data of memory cells read from the memory cell array 1 are outputted to the outside from the data input-output terminal 5 via the bit line control circuit 2, the data input-output buffer 4, and the controller 11. The memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input-output buffer 4, a word line control circuit 6, and a control signal input terminal 8 constitute a nonvolatile semiconductor storage device 100, and the controller 11 and the data input-output terminal 5 are added to this to constitute a nonvolatile semiconductor storage system. Furthermore, write data inputted to the data input-output terminal 5 from the outside are inputted to the bit line control circuit 2 by the column decoder 3 via the data input-output buffer 4, and

writing to a designated memory cell is carried out.

[0024]

In addition, the memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input-output buffer 4, the word line control circuit 6, and the controller 11 are connected to the control circuit 7. According to a control signal inputted to the control signal input terminal 8, the control circuit 7 generates a control signal and control voltage for controlling the memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input-output buffer 4, the word line control circuit 6, and the controller 11.

[0025]

In the read operation, the word line control circuit 6 performs control to apply multi-bit data read voltage or verify voltage between one upper limit among four pieces of threshold distribution of four-valued data (FIG. 1) and the lower limit of another piece of threshold distribution having larger values (VA, VB and VC in FIG. 1) to the word line WL as word line voltage.

[0026]

In addition to this, the word line control circuit 6 performs, for generation of a soft value which is discussed below, control to apply a plurality of voltages having magnitudes between the upper limit and the lower limit of each of the four pieces of threshold distribution (soft value read voltages) to the word line WL as word line voltage. The details will be discussed below.

(Omitted)

[0033]

FIG. 5 indicates the constitution of the memory cell array 1 and the bit line control circuit 2 shown in FIG. 1. The memory cell array 1 is a NAND cell memory cell array, and is constituted to include a plurality of NAND cells. One NAND cell includes a memory cell MC composed of 16 series-connected EEPROMs, for example, and selection gates S1, S2 connected to respective ends of the memory cell MC. The selection gate S1 is connected to a bit line BL0, and the selection gate S2 is connected to a source line SRC.

[0034]

Control gates of pieces of the memory cell MC arranged in an identical row are commonly connected to the word lines WL1, WL2, WL3...WL16. In addition, the first selection gate S1 is commonly connected to a select line SG1, and a second selection gate S2 is commonly connected to a select line SG2.

[0035]

The memory cell array 1 includes a plurality of blocks as shown in the broken lines. Each block includes a plurality of NAND cells, and data are deleted in units of such blocks. In addition, the deletion operation is carried out with respect to two bit lines connected to the data storing circuit 10 and the flag data storing circuit 10a at the same time.

[0036]

The bit line control circuit 2 has a plurality of pieces of data storing circuit 10 and a flag data storing circuit 10a. To each piece of the data storing circuit 10 and the flag data storing circuit 10a, a pair of bit lines (BL0, BL1), (BL2, BL3)...(BLi, BLi+1), (BL, BL) are connected. Each piece of data storing circuit 10 has a function to hold data read from the memory cell MC as well as a function to hold data to be written in the memory cell MC. In addition, it has a role to manipulate internal data on the occasion of performing multi-bit data storing and multi-bit data reading as will be mentioned later, and on the occasion of performing soft value data generation as will also be mentioned later.

[0037]

Furthermore, a plurality of memory cells arranged in every other bit line BLi and connected to one piece of word line WLi (memory cells in a range surrounded with the broken line) constitute one sector. Data are written and read for each sector. In one sector, data corresponding to two pages are stored, for example. In addition, to each word line WL, a flag cell FC for storing flag data FLAG is connected. As previously explained, flag data FLAG stored in this flag cell FC is made to be '1' at a stage when a write operation of low order page data to the memory cell MC has ended, and made to be '0' at a stage when writing of high order page data has finished.

[0038]

At the time of a read operation, a program verify operation, and a program operation, one bit line is selected from two bit lines (BLi, BLi+1) connected to the data storing circuit 10 in accordance with an address signal (flags YA1, YA2...YAi, YAflag) designated from the outside. Moreover, in accordance with an external address, one word line is selected to select one sector (this corresponds to two pages). Switching of such two pages is made by an address.

(Omitted)

[0041]

FIG. 8 indicates a cross section of one NAND cell of a memory cell array. In this example, one NAND cell is constituted in a manner that 16 pieces of memory cell MC of the configuration shown in FIG. 6 are series-connected. In the drain side and the

source side of a NAND cell, first selection gates S1 and S2 of the configuration shown in FIG. 7 are provided.

[0042]

A configuration example of the data storing circuit 10 will be described by reference to FIG. 9. Meanwhile, a configuration of the data storing circuit 10a is similar to it, and thus description will be omitted. The data storing circuit 10 has a primary data cache (PDC), a secondary data cache (SDC), a dynamic data cache (DDC), and a temporary data cache (TDC).

[0043]

The SDC, PDC, DDC are responsible for holding input data at the time of write, for holding read data on the occasion of read, for holding data on a temporary basis on the occasion of verifying, and for data storage for handling internal data when storing multi-bit data. The TDC is used for amplifying data of a bit line on the occasion of data read, for holding the amplifying data on a temporary basis, and for handling internal data when storing multi-bit data.

[0044]

The SDC includes clocked inverter circuits 61a, 61b, and transistors 61c, 61d, which constitute a latch circuit. The transistor 61c is connected between the input port of the clocked inverter circuit 61a and the input port of the clocked inverter circuit 61b, and a signal EQ2 is supplied to its gate."

B" [0070]

[Read operation]

Next, usual read operations of four-valued data will be described in a manner being divided into reading of low order page data and reading of high order page data.

[0071]

FIG. 12 indicates a read procedure of low order page data by a flowchart. First, an address is designated to select one sector shown in FIG. 5. Next, a read operation is performed in a manner making a potential of the selected word line be VA (S31), and whether flag data FLAG of the flag cell FC is '0' or '1' is determined (S32).

[0072]

In the case of flag data FLAG read from the flag cell FC being '1', writing of high order page data has not finished yet, and, for this reason, the threshold voltage distribution of the memory cell MC is as shown in FIG. 2. A read operation for this data should just be performed in a manner making the potential of a word line be VA, and, accordingly, the data have been already read into the data storing circuit 10. For

this reason, the data stored in the data storing circuit 10 are outputted to the outside to perform reading (S33).

[0073]

On the other hand, in the case of flag data FLAG read from the flag cell FC being '0' (data of the memory cell are '1'), writing of high order page data has been already performed, and, therefore, the threshold voltage distribution of the memory cell MC is as shown in FIG. 3. Accordingly, a read operation is performed by setting the potential of the word line to VB (S34), and, after this, data read to the data storing circuit 10 are outputted to the outside (S33). Operations of each data cache in the data storing circuit 10 on this occasion are approximately similar to those on the occasion of the write verify operation.

[0074]

Next, a procedure of a read operation of high order page data will be described by reference to the flowchart of FIG. 13. In reading of high order page data, an address is designated, first, and one sector shown in FIG. 5 is selected. Next, reading is performed making the potential of a word line be VC (S35). By this, '1' is read from a memory cell having a threshold voltage lower than VC, '0' is read from a memory cell having a threshold voltage higher than VC, and the read data are held in the TDC as temporary high order page data Upper (pre1). The data Upper (pre1) held in TDC is forwarded to PDC by a transistor 61h being made to be ON once, and, after that, is held in DDCA by a transistor 61sA being made to be ON.

[0075]

After that, a read operation is performed in a way making the word line potential be VA (S36), and whether flag data FLAG of the flag cell FC is '0' or '1' is determined (S37).

[0076]

As a result, when flag data FLAG of the flag cell FC is '1' and writing of high order page has not been carried out yet, output data are fixed to '1' (S38). In order to make the output be '1', signal PRST of the data storing circuit 10 is made to be 'H', and SDC is set to '1'. Alternatively, the data input-output buffer 4 is made to output only data '1'.

[0077]

In addition, in the case of flag data FLAG of the flag cell being '0', high order page data Upper is read based on the data Upper (pre1) held in DDCA, and data Upper (pre2) to be read newly (S39). Specific operations of the data storing circuit 10 in this read will be described hereinafter.

[0078]

Newly read data Upper (pre2) is held in TDC. On this occasion, in a state that VPRE is made to be the ground potential, signal REGA of the gate of a transistor 61qA is made to be 'H'. On this occasion, when the data Upper (pre1) held in DDCA is '0'; that is, when the potential of the gate of a transistor 61rA is 'H', the voltage of the node N3 is discharged. On the other hand, when the data Upper (pre1) held in DDCA is '1'; that is, when the potential of the gate of the transistor 61rA is 'L', the voltage of the node N3 is not changed. In other words, in the case where the data Upper (pre1) held in DDCA is '0', new data Upper (pre2) is forced to be reversed to '1'.

[0079]

The data held in TDC after performing the operation mentioned above are transferred to SDC and then outputted to the outside as high order page data Upper. The relation between the data Upper (pre1) and the high order page data Upper to be outputted is as shown in FIG. 14. The low order page data Lower and the high order page data Upper are read by the procedure as above, and the reading of the four-valued data is completed."

C "[0082]

In this FIG. 15, each of the soft value read voltages (4)-(7) is voltage in the vicinity of the middle point (almost the intermediate point between the upper limit and the lower limit) of each piece of threshold distribution of data '11', '01', '10', and '00'. In addition, the other soft value read voltages (8)-(15) are being set to voltages to make each threshold distribution be divided at almost regular intervals with soft value read voltages (4)-(7). That is,

(i) soft value read voltages (4), (8), (9) are being set so as to divide the threshold distribution of data '00' at approximately regular intervals,

(ii) soft value read voltages (5), (10), (11) are being set so as to divide the threshold distribution of data '10' at approximately regular intervals,

(iii) soft value read voltages (6), (12), (13) are being set so as to divide the threshold distribution of data '00' at approximately regular intervals, and

(iv) soft value read voltages (7), (14), (15) are being set so as to divide the threshold distribution of data '11' at approximately regular intervals.

[0083]

This is an example when threshold distribution is supposed to be approximately a shape of Gaussian distribution, and read voltage setting is not limited to this example. Due to a shape of distribution, division may be made in distorted intervals to a certain

degree in each piece of threshold distribution. In addition, the number of pieces of division of each piece of threshold distribution; that is, the number of soft value read voltages included in each piece of threshold distribution, may be 4 or more without being limited to 3.

[0084]

Next, the specific generation procedure of such soft value data will be described by reference to FIG. 15. First, as has been described using FIG. 12 and FIG. 13, the word line voltage is set to (1) multi-bit data read voltage VB, (2) multi-bit data read voltage VC, and (3) multi-bit data read voltage VA in turn, and low order page data Lower, temporary high order page data Upper (pre1), and high order page data Upper are read.

[0085]

The matrix expression of '1' and '0' described in the lower half of FIG. 15 indicates the magnitude of a threshold voltage of the memory cell in question, and page data and a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2) that can be obtained, when the word line voltage is made to be changed to (1), (2), ..., (15).

[0086]

Next, the word line voltage is set to soft value read voltages (4)-(7) in the vicinity of the intermediate point between the upper limit and the lower limit of each piece of threshold distribution in that order (that is, in a stepwise manner decreasing from the highest to the lowest). First, soft value data soft value 1 (pre1) that is read when soft value read voltage (4) is set is read as data '0' about only memory cells having a threshold voltage greater than the right half of the threshold distribution of data '00', and the others are read as '1'. This soft value 1 (pre1) that has been read is held in TDC once, and then held in DDCA via PDC.

[0087]

Next, soft value read voltage (5) is set to read soft value data soft value 1 (pre2). This soft value 1 (pre2) is read as data '0' only about memory cells having a threshold voltage greater than the right half of the threshold distribution of data '10', and all the rest are read as '1' and held in TDC. In this regard, however, soft value 1 (pre1) is being held in DDCA, and, if soft value 1 (pre1) being held in DDCA is '0', the data held in TDC are forced to be made to be reversed to '1' (refer to the arrow in FIG. 15). In other words, as soft value read voltage is made to be smaller in a stepwise manner, if both of a first soft value read voltage and a second soft value read voltage that is smaller than the former by one step have not made a memory cell be conducted, data obtained by the

second soft value read voltage are reversed and is made to be a soft value.

[0088]

Hereinafter, in a similar fashion, soft value read voltages (6), (7) are applied as word line voltages, and, when soft value 1 (prei) just before is '0', data reverse is performed. Data generated by soft value read voltage (7) is soft value 1, and it is used for likelihood calculation in the likelihood calculation circuit 102 along with soft value 2 which is discussed below.

[0089]

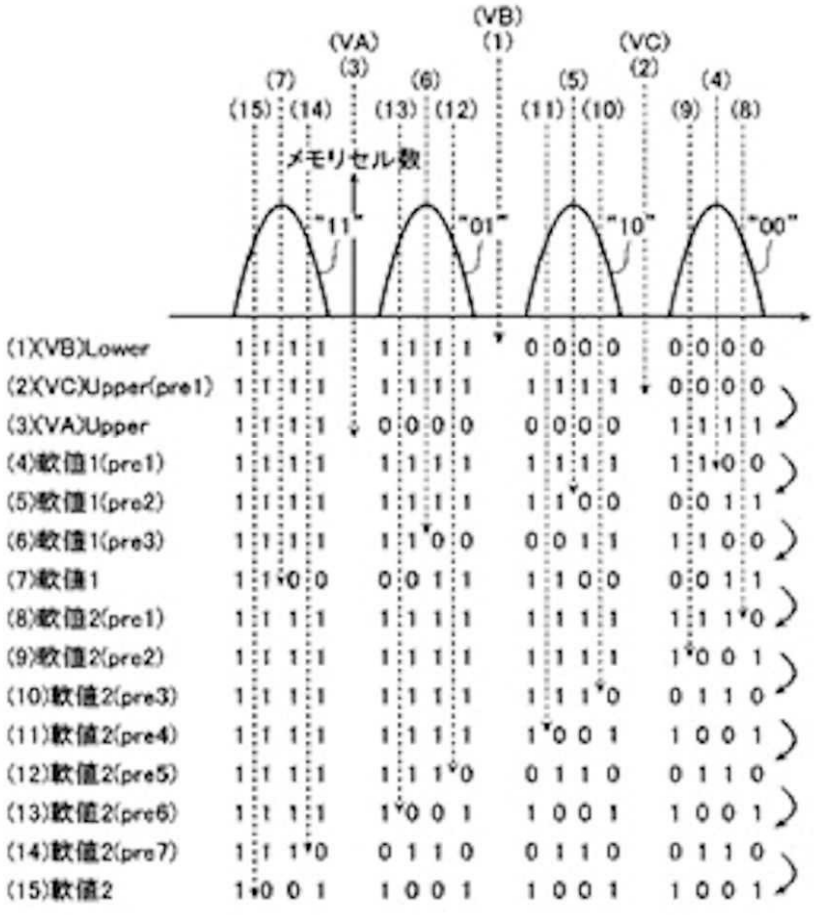
Next, word line voltage is set to soft value read voltages (8)-(15) in that order (that is, in a stepwise manner decreasing from the highest to the lowest). A point that data reverse is made when a previous soft value held in DDCA is '0' is similar to that in the case of (4)-(7). Soft value 2 generated by applying soft value read voltage (15) as word line voltage is used for the purpose of likelihood calculation in the likelihood calculation circuit 102 in conjunction with soft value 1.

[0090]

In a nonvolatile semiconductor storage device of the present embodiment, in parallel with execution of the above-mentioned soft value generation procedure, it is possible to carry out error detection and error correction by the first error correction circuit 101 based on multi-bit data having been obtained in advance of soft value acquisition and redundant data. When all errors have been corrected as a result of error detection/correction in the first error correction circuit 101, a soft value having been generated in parallel becomes unnecessary and is deleted, and corrected data by the first error correction circuit 101 are outputted from the output control circuit 104. When it is determined as error correction by the first error correction circuit 101 based on redundant data having failed, the second error correction circuit 103 starts error correction based on, in addition to multi-bit data and redundant data, likelihood having been calculated by the likelihood calculation circuit 102 using a soft value. By execution of such parallel processing, it is possible to realize throughput improvement of data transfer."

D FIG. 15

【図１５】



メモリセル数	The number of memory cells
軟値１	Soft value 1

(2-2) Finding of the Cited Invention

(A) It is recognized that there is described in Cited Document 1 "a nonvolatile semiconductor storage system including a NAND cell flash memory to store four values", because there is described in the above-mentioned A that "the present invention relates to a nonvolatile semiconductor storage system, and, more particularly, to a nonvolatile semiconductor storage system provided with a nonvolatile semiconductor device capable of storing two or more bits of data (multi-bit data) in one memory cell. (Omitted) FIG. 4 illustrates a configuration of a system provided with NAND cell flash memory to store four values (2 bits) as an example of a nonvolatile semiconductor

storage system".

(B) Since there is described in the above-mentioned A that "This flash memory includes a memory cell array 1 configured by arranging memory cells to store data in matrix. The memory cell array 1 includes a plurality of bit lines, a plurality of word lines, and a common source line, and electrically data-rewritable memory cells are arranged in matrix at intersection points of the bit lines and the word lines", it is recognized that there is described in "a nonvolatile semiconductor storage system" of Cited Document 1 "a memory cell array configured by arranging memory cells to store data in matrix".

(C) There is described in the above-mentioned A that "the memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input-output buffer 4, the word line control circuit 6 and the controller 11 are connected to the control circuit 7. According to a control signal inputted to the control signal input terminal 8, the control circuit 7 generates a control signal and control voltage for controlling the memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input-output buffer 4, the word line control circuit 6 and the controller 11.". Therefore, it is recognized that there is described in "a nonvolatile semiconductor storage system" of Cited Document 1 "a control circuit to make a control signal and control voltage for controlling a memory cell array, a bit line control circuit, a column decoder, a data input-output buffer, a word line control circuit, and a controller be generated".

(D) There is described in the above-mentioned A that "the memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input-output buffer 4, the word line control circuit 6 and the controller 11 are connected to the control circuit 7. According to a control signal inputted to the control signal input terminal 8, the control circuit 7 generates a control signal and control voltage for controlling the memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input-output buffer 4, the word line control circuit 6, and the controller 11.". Therefore, it can be said that there is described in Cited Document 1 that "the control circuit generates a control signal and control voltage for controlling a memory cell array and a bit line control circuit".

There is described in the above-mentioned A that "Each piece of data storing circuit 10 has a function to hold data read from the memory cell MC as well as a function to hold data to be written in the memory cell MC. In addition, it has a role to manipulate internal data on the occasion of performing multi-bit data storing and multi-bit data reading as will be mentioned later, and on the occasion of performing soft value

data generation as will be also mentioned later", and in the above-mentioned B that "FIG. 13 indicates the read procedure of low order page data by a flowchart. First, an address is designated to select one sector shown in FIG. 5. (Omitted) A read operation for this data should just be performed in a manner making the potential of a word line be VA, and, accordingly, the data have been already read into the data storing circuit 10. For this reason, the data stored in the data storing circuit 10 are outputted to the outside to perform read. (Omitted) Next, the procedure of a read operation of high order page data will be described by reference to the flowchart of FIG. 13. In read of high order page data, an address is designated, first, and one sector shown in FIG. 5 is selected. (Omitted) The data held in TDC after performing the operation mentioned above are transferred to SDC and then outputted to the outside as high order page data Upper". Therefore, it can be said that there is described in Cited Document 1 "a data storing circuit to, following a read procedure: designate an address to select a sector; read high order page data, low order page data, and soft value data; and output the high order page data, the low order page data, and the soft value data as a read result".

There is described in the above-mentioned C that "The matrix expression of '1' and '0' described in the lower half of FIG. 15 indicates the magnitude of a threshold voltage of the memory cell in question, and page data and a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2) that can be obtained, when the word line voltage is made to be changed to (1), (2), ..., (15)". Therefore, it can be said that soft value data includes "a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2)", and, therefore, it can be said that there is described in Cited Document 1 "a data storing circuit to read low order page data, high order page data, and a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2)".

From the above, it is recognized that there is described in "a nonvolatile semiconductor system" of Cited Document 1,
"a data storing circuit in which a control circuit generates a control signal and control voltage for controlling a memory cell array and a bit line control circuit, and, following a read procedure, designates an address to select a sector, reads low order page data, high order page data, and a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2), and outputs the low order page data, high order page data, soft value 1 and soft value 2 as a read result".

(E) There is described in the above-mentioned A that "the memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input-output buffer 4, the word line control circuit 6, and the controller 11 are connected to the control circuit 7. According

to a control signal inputted to the control signal input terminal 8, the control circuit 7 generates a control signal and control voltage for controlling the memory cell array 1, the bit line control circuit 2, the column decoder 3, the data input-output buffer 4, the word line control circuit 6, and the controller 11". Therefore it can be said that there is described in Cited Document 1 that "a control circuit generates control signal and control voltage for controlling a word line control circuit."

There is described in the above-mentioned A that "In the read operation, the word line control circuit 6 performs control to apply multi-bit data read voltage or verify voltage between one upper limit among four pieces of threshold distribution of four-valued data (FIG. 1) and the lower limit of another piece of threshold distribution having larger values (VA, VB and VC in FIG. 1) to the word line WL as word line voltage". Therefore, there is described in Cited Document 1 "a word line control circuit to make the potential of a selected word line be a threshold voltage in order to read data".

There is described in the above-mentioned C that "Next, a specific generation procedure of such soft value data will be described by reference to FIG. 15. First, as has been described using FIG. 12 and FIG. 13, the word line voltage is set to (1) multi-bit data read voltage VB, (2) multi-bit data read voltage VC, and (3) multi-bit data read voltage VA in turn, and low order page data Lower, temporary high order page data Upper (pre1), and high order page data Upper are read. (Omitted) The matrix expression of '1' and '0' described in the lower half of FIG. 15 indicates the magnitude of a threshold voltage of the memory cell in question, and page data and a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2) that can be obtained, when the word line voltage is made to be changed to (1), (2), ..., (15)". Therefore, it can be said that there is described in Cited Document 1 "a word line control circuit to make the potential of a selected word line be a threshold voltage in order to read low order page data, high order page data, and a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2)".

From the above, it is recognized that there is described in "a nonvolatile semiconductor system" of Cited Document 1 "a word line control circuit in which a control circuit generates a control signal and control voltage for controlling the word line control circuit, and makes the potential of a selected word line be a threshold voltage in order to read low order page data, high order page data, and a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2)".

(F) From the statements in the above-mentioned C that "the word line voltage is set to

soft value read voltages (4)-(7) in the vicinity of the intermediate point between the upper limit and the lower limit of each piece of threshold distribution in that order (that is, in a stepwise manner decreasing from the highest to the lowest). First, soft value data soft value 1 (pre1) that is read when soft value read voltage (4) is set is read as data '0' about only memory cells having a threshold voltage greater than the right half of the threshold distribution of data '00', and the others are read as '1'. This soft value 1 (pre1) that has been read is held in TDC once, and then held in DDCA via PDC. (Omitted) Next, soft value read voltage (5) is set to read soft value data soft value 1 (pre2). This soft value 1 (pre2) is read as data '0' only about memory cells having a threshold voltage greater than the right half of the threshold distribution of data '10', and all the rest are read as '1' and held in TDC. In this regard, however, soft value 1 (pre1) is being held in DDCA, and, if soft value 1 (pre1) being held in DDCA is '0', the data held in TDC is forced to be made to be reversed to '1' (refer to the arrow in FIG. 15). (Omitted) Hereinafter, in a similar fashion, soft value read voltages (6), (7) are applied as word line voltages, and, when soft value 1 (prei) just before is '0', data reverse is performed. Data generated by soft value read voltage (7) is soft value 1, and it is used for likelihood calculation in the likelihood calculation circuit 102 along with soft value 2 which is discussed below. (Omitted) In a nonvolatile semiconductor storage device of the present embodiment, in parallel with execution of the above-mentioned soft value generation procedure, it is possible to carry out error detection and error correction by the first error correction circuit 101 based on multi-bit data having been obtained in advance of soft value acquisition and redundant data" and from the statement of FIG. 15 of the above-mentioned D, it is recognized that there is described in Cited Document 1 that "soft value 1 (pre1) to soft value 1 (pre3) are read by applying soft value read voltages (4)-(7) in the vicinity of the intermediate point between the upper limit and the lower limit of each piece of threshold distribution in that order (that is, in a stepwise manner decreasing from the highest to the lowest) as a word line voltage, and soft value 1 generated by the soft value read voltage (7) is generated by execution of soft value generation procedure and outputted".

(G) From the statements of the above-mentioned C that "Next, word line voltage is set to soft value read voltages (8)-(15) in that order (that is, in a stepwise manner decreasing from the highest to the lowest). A point that data reverse is made when a previous soft value held in DDCA is '0' is similar to that in the case of (4)-(7). Soft value 2 generated by applying soft value read voltage (15) as word line voltage is used for the purpose of likelihood calculation in the likelihood calculation circuit 102 in

conjunction with soft value 1" and from the examination of the above (F), it is recognized that there is described in Cited Document 1 that
"soft value 2 (pre1) to soft value 2 (pre7) are read by applying soft value read voltages (8)-(15) in that order (that is, in a stepwise manner decreasing from the highest to the lowest) to the word line, and soft value 2 generated by soft value read voltage (15) as a word line voltage is generated by execution of a soft value generation procedure and outputted".

(H) In the above-mentioned A, there is described that "Each piece of data storing circuit 10 has a function to hold data read from the memory cell MC as well as a function to hold data to be written in the memory cell MC", and also in the above-mentioned A there is described that "A configuration example of the data storing circuit 10 will be described referring to FIG. 9. Meanwhile, a configuration of the data storing circuit 10a is similar to it, and thus description will be omitted. The data storing circuit 10 has a primary data cache (PDC), a secondary data cache (SDC), a dynamic data cache (DDC), and a temporary data cache (TDC).", and, therefore, it is recognized that there is described in Cited Document 1 that "each data storing circuit has a function to hold data to be read from a memory cell, and includes a primary data cache (PDC), a secondary data cache (SDC), a dynamic data cache (DDC), and a temporary data cache (TDC)".

(I) Since there is described in the above-mentioned C that "The data held in TDC after performing the operation mentioned above are transferred to SDC and then outputted to the outside as high order page data Upper", it is recognized that there is described in Cited Document 1 that "each data storing circuit has SDC to output, after performing a page data read operation, holding data of TDC to the outside after the data have been transferred to SDC".

(J) Since there is described in the above-mentioned C that "the word line voltage is set to soft value read voltages (4)-(7) in the vicinity of the intermediate point between the upper limit and the lower limit of each piece of threshold distribution in that order (that is, in a stepwise manner decreasing from the highest to the lowest). First, soft value data soft value 1 (pre1) that is read when soft value read voltage (4) is set is read as data '0' about only memory cells having a threshold voltage greater than the right half of the threshold distribution of data '00', and the others are read as '1'. This soft value 1 (pre1) that has been read is held in TDC once, and then held in DDCA via PDC. (Omitted) Next, soft value read voltage (5) is set to read soft value data soft value 1 (pre2). This

soft value 1 (pre2) is read as data '0' only about memory cells having a threshold voltage greater than the right half of the threshold distribution of data '10', and all the rest are read as '1' and held in TDC. In this regard, however, soft value 1 (pre1) is being held in DDCA, and, if soft value 1 (pre1) being held in DDCA is '0', the data held in TDC are forced to be made to be reversed to '1' (refer to the arrow in FIG. 15). (Omitted) Hereinafter, in a similar fashion, soft value read voltage (6), (7) are applied as word line voltages, and, when soft value 1 (prei) just before is '0', data reverse is performed. Data generated by soft value read voltage (7) is a soft value 1, and it is used for likelihood calculation in the likelihood calculation circuit 102 along with soft value 2 which is discussed below. (Omitted) Next, word line voltage is set to soft value read voltages (8)-(15) in that order (that is, in a stepwise manner decreasing from the highest to the lowest). A point that data reverse is made when a previous soft value held in DDCA is '0' is similar to that in the case of (4)-(7). Soft value 2 generated by applying soft value read voltage (15) as word line voltage is used for the purpose of likelihood calculation in the likelihood calculation circuit 102 in conjunction with soft value 1. (Omitted) In a nonvolatile semiconductor storage device of the present embodiment, in parallel with execution of the above-mentioned soft value generation procedure, it is possible to carry out error detection and error correction by the first error correction circuit 101 based on multi-bit data having been obtained in advance of soft value acquisition and redundant data", it is recognized that there is described in "a data storing circuit" of Cited Document 1 that "read voltages ((4)-(7), (8)-(15)) are applied to a word line, data are read as '0' about memory cells having larger threshold voltages, and about all the rest data are read as '1', the data are held in TDC, the data held in TDC is forcibly reversed to '1' when soft value 1 (prei) to soft value 2 (prei) previously held in DDC are '0', TDC and DDC in which soft value 1 and soft value 2 are generated by execution of the soft value generation procedure are provided, and soft value 1 and soft value 2 are generated by holding soft value 1 (pre1) to soft value 1 (pre3) and soft value 2 (pre1) to soft value 2 (pre7) in TDC and DDC and by executing a soft value generation procedure".

(K) From the examination of the above-mentioned (A) to (J), it is recognized that there is described in Cited Document 1 the following invention (hereinafter, referred to as "the Cited Invention").

"A nonvolatile semiconductor storage system including a NAND cell flash memory to store four values, comprising:

a memory cell array configured by arranging memory cells to store data in

matrix;

a control circuit to make a control signal and control voltage for controlling the memory cell array, a bit line control circuit, a column decoder, a data input-output buffer, a word line control circuit, and a controller be generated;

a data storing circuit to output low order page data, high order page data, soft value 1, and soft value 2 as read result by the control circuit generating a control signal and control voltage for controlling the memory cell array and the bit line control circuit and, following a read procedure, designating an address to select a sector, and reading the low order page data, the high order page data, and the soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2); and

a word line control circuit to make potential of a selected word line be a threshold voltage by the control circuit generating a control signal and control voltage for controlling the word line control circuit in order to read the low order page data, the high order page data, and the soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2), wherein

soft value 1 (pre1) to soft value 1 (pre3) are read by applying soft value read voltages (4)-(7) in the vicinity of the intermediate point between the upper limit and the lower limit of each piece of threshold distribution in that order (that is, in a stepwise manner decreasing from the highest to the lowest) as a word line voltage, and soft value 1 generated by the soft value read voltage (7) is generated by execution of soft value generation procedure and outputted, wherein

soft value 2 (pre1) to soft value 2 (pre7) are read by applying soft value read voltages (8)-(15) in that order (that is, in a stepwise manner decreasing from the highest to the lowest) to the word line, and soft value 2 generated by soft value read voltage (15) as a word line voltage is generated by execution of a soft value generation procedure and outputted, wherein

each data storing circuit has a function to hold data to be read from a memory cell, and includes a primary data cache (PDC), a secondary data cache (SDC), a dynamic data cache (DDC), and a temporary data cache (TDC), wherein

each data storing circuit has SDC to output, after performing a page data read operation, holding data of TDC to the outside after the data have been transferred to SDC, wherein

TDC and DDC in which read voltages ((4)-(7), (8)-(15)) are applied to the word line, data are read as '0' about memory cells having larger threshold voltages, data are read as '1' about all the rest, the data are held in TDC, the data held in TDC are forcibly reversed to '1' when soft value 1 (prei) to soft value 2 (prei) previously held in DDC are

'0', and soft value 1 and soft value 2 are generated by execution of the soft value generation procedure, and wherein

soft value 1 and soft value 2 are generated by holding soft values 1 (pre1) to (pre3) and soft values 2 (pre1) to (pre7) in TDC and DDC and by executing a soft value generation procedure."

(3) Comparison

The Amended Invention and the Cited Invention are compared.

(A) A "nonvolatile semiconductor storage system including a NAND cell flash memory to store four values" in the Cited Invention corresponds to a "flash memory device" in the Amended Invention.

(B) It is obvious that "a memory cell array" of the Cited Invention includes a plurality of memory cells because it is "arranging memory cells in matrix", and, therefore, "a memory cell array configured by arranging memory cells to store data in matrix" in the Cited Invention corresponds to "a memory cell array including a plurality of memory cells" in the Amended Invention.

(C) When "A control circuit to make a control signal and control voltage for controlling the memory cell array, a bit line control circuit, a column decoder, a data input-output buffer, a word line control, circuit and a controller be generated" in the Cited Invention and "a control logic configured to control a read operation on the plurality of memory cells" in the Amended Invention are compared, "control circuit" of the Cited Invention generates a control signal and control voltage for controlling "memory cell array" and "bit line control circuit", and "memory cell array" and "bit line control circuit" of the Cited Invention have a function to read data of a memory cell in a memory cell array via a bit line, and, thus, "control circuit" of the Cited Invention corresponds to "control logic" of the Amended Invention.

Then, there is no substantial difference between the two.

(D) When "a data storing circuit to output low order page data, high order page data, soft value 1, and soft value 2 as read result by the control circuit generating a control signal and control voltage for controlling the memory cell array and the bit line control circuit and, following a read procedure, designating an address to select a sector, and reading the low order page data, the high order page data, and the soft value (soft value

1 (prei), soft value 2 (prei), soft value 1, soft value 2)" in the Cited Invention and "a page buffer circuit configured to sense hard decision data and a plurality of soft decision data from each of a plurality of selected memory cells in response to the control of the control logic and output the sensed hard decision data and the plurality of soft decision data as a read result" in the Amended Invention are compared, "low order page data, high order page data" of the Cited Invention correspond to "hard decision data" of the Amended Invention, "soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2)" of the Cited Invention corresponds to "soft decision data" of the Amended Invention, reading data by "the control circuit 7 generating a control signal and control voltage for controlling a memory array and a bit line control circuit" of the Cited Invention corresponds to sensing data "in response to the control of the control logic" of the Amended Invention. Therefore, it can be said that "data storing circuit" of the Cited Invention corresponds to "page buffer circuit" of the Amended Invention.

Accordingly, there is no substantial difference between the two.

(E) When " a word line control circuit in which a control circuit generates a control signal and control voltage for controlling the word line control circuit, and makes the potential of a selected word line be a threshold voltage in order to read low order page data, high order page data, and a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2)" in the Cited Invention and "a voltage generation circuit configured to generate a plurality of read voltages for reading the hard decision data and the plurality of soft decision data in response to the control of the control logic" in the Amended Invention are compared,

it can be said that "low order page data, high order page data" of the Cited Invention correspond to "hard decision data" of the Amended Invention, "a soft value (soft value 1 (prei), soft value 2 (prei), soft value 1, soft value 2)" of the Cited Invention correspond to "soft decision data" of the Amended Invention, and making potential of a selected word line to a threshold voltage by "the control circuit generating a control signal and control voltage for controlling the word line control circuit" of the Cited Invention corresponds to generating a plurality of read voltages "in response to the control of the control logic" of the Amended Invention, and, therefore, "a word line control circuit" of the Cited Invention corresponds to "a voltage generation circuit" of the Amended Invention.

Then, there is no substantial difference between the two.

(F) When "soft value 1 (pre1) to soft value 1 (pre3) are read by applying soft value read

voltages (4)-(7) in the vicinity of the intermediate point between the upper limit and the lower limit of each piece of threshold distribution in that order (that is, in a stepwise manner decreasing from the highest to the lowest) as a word line voltage" and "soft value 2 (pre1) to soft value 2 (pre7) are read by applying soft value read voltages (8)-(15) in that order (that is, in a stepwise manner decreasing from the highest to the lowest) to a word line" in the Cited Invention and "the plurality of soft decision data are sensed between adjacent pieces of threshold voltage distribution" in the Amended Invention are compared,

"soft value 1 (pre1) to soft value 1 (pre3)" and "soft value 2 (pre1) to soft value 2 (pre7)" of the Cited Invention correspond to "a plurality of soft decision data" of the Amended Invention, and "soft value read voltages (4)-(7) in the vicinity of the intermediate point between the upper limit and the lower limit of each piece of threshold distribution" and "soft value read voltages (8)-(15)" of the Cited Invention are applied in that order (that is, in a stepwise manner decreasing from the highest to the lowest) to a word line voltage. Therefore, it can be said that they are adjacent threshold voltages (threshold voltages), and, thus, the matter that "soft value 1 (pre1) to soft value 1 (pre3)" and "soft value 2 (pre1) to soft value 2 (pre7)" "are read" of the Cited Invention can be said to correspond to "being sensed between adjacent pieces of threshold voltage distribution" of the Invention.

Then, there is no substantial difference between the two.

(G) When "soft value 1 (pre1) to soft value 1 (pre3) are read by applying soft value read voltages (4)-(7) in the vicinity of the intermediate point between the upper limit and the lower limit of each piece of threshold distribution in that order (that is, in a stepwise manner decreasing from the highest to the lowest) as a word line voltage, and soft value 1 generated by the soft value read voltage (7) is generated by execution of soft value generation procedure and outputted " and "soft value 2 (pre1) to soft value 2 (pre7) are read by applying soft value read voltages (8)-(15) in that order (that is, in a stepwise manner decreasing from the highest to the lowest) to the word line, and soft value 2 generated by soft value read voltage (15) as a word line voltage is generated by execution of a soft value generation procedure and outputted" in the Cited Invention and "the plurality of soft decision data included in the read result are encoded into reliability data to be outputted" in the Amended Invention are compared,

"soft value 1 (pre1) to soft value 1 (pre3)" and "soft value 2 (pre1) to soft value 2 (pre7)" of the Cited Invention correspond to "soft decision data" of the Amended Invention, and are read by read voltages ((4)-(7), (8)-(15)) being applied to a word line,

and, thus, it can be said that they are included in a read result, and "soft value 1" and "soft value 2" of the Cited Invention correspond to "reliability data" of the Amended Invention. In general, it can be understood as "encoding" is converting in accordance with a given rule, and, thus, it can be said that being generated (converted) by execution of a soft value generation procedure is encoding.

Then, there is no substantial difference between the two.

(H) The expression "Each data storing circuit has a function to hold data to be read from a memory cell, and includes a primary data cache (PDC), a secondary data cache (SDC), a dynamic data cache (DDC), and a temporary data cache (TDC)" in the Cited Invention corresponds to the expression "the page buffer circuit includes a plurality of page buffers corresponding respectively to the selected memory cells" in the Amended Invention.

(I) The expression "data are read as '0' about memory cells having larger threshold voltages, and about all the rest data are read as '1', the data are held in TDC." of the Cited Invention corresponds to "being latched in response to values of the soft decision data" of the Amended Invention, and it can be said that, regarding that "the data held in TDC is forcibly reversed to '1' when soft value 1 (prei) previously held in DDC is '0'" of the Cited Invention, to reverse a value held in TDC to '1' from '0' is identical with being toggled, and "TDC and DDC" of the Cited Invention correspond to "a first type latch" of the Amended Invention.

Furthermore, "SDC to output holding data of TDC to the outside as high order page data Upper after the data has been transferred to SDC" in the Cited Invention corresponds to "a second type latch to latch hard decision data" in the Amended Invention because "high order page data Upper" of the Cited Invention corresponds to "hard decision data" of the Amended Invention, and "SDC" of the Cited Invention corresponds to "second type latch" of the Amended Invention.

Consequently, the description "each data storing circuit has SDC to output, after performing a page data read operation, holding data of TDC to the outside after the data has been transferred to SDC, wherein TDC and DDC in which read voltages ((4)-(7), (8)-(15)) are applied to the word line, data are read as '0' about memory cells having larger threshold voltages, data are read as '1' about all the rest, the data are held in TDC, the data held in TDC is forcibly reversed to '1' when soft value 1 (prei) to soft value 2 (prei) previously held in DDC are '0', and soft value 1 and soft value 2 are generated by execution of the soft value generation procedure" in the Cited Invention corresponds to

"each of the page buffers includes a plurality of first type latches to encode the reliability data by values latched in response to values of the plurality of soft decision data being toggled and a second type latch to latch the hard decision data" in the Amended Invention.

(J) When "soft value 1 and soft value 2 are generate by holding soft values 1 (pre1) to (pre3) and soft values 2 (pre1) to (pre7) in TDC and DDC and by executing a soft value generation procedure" in the Cited Invention and "the reliability data are expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data by being encoded in the plurality of first type latches" of the Amended Invention are compared,

since it can be said that "TDC" and "DDC" of the Cited Invention correspond to "first type latch" of the Amended Invention, are included in a data storing circuit, perform latching of "soft value 1 (pre1) to soft value 1 (pre3)" and "soft value 2 (pre1) to soft value 2 (pre7)", and a soft value is generated (encoded) by a soft value generation procedure, the two are identical in a point that "reliability data are encoded in the plurality of first type latches".

(K) From the above-mentioned examination of (A) to (J), the Amended Invention and the Cited Invention are identical and different in the following points.

<Corresponding features>

A flash memory device comprising:

a memory cell array including a plurality of memory cells;

a control logic configured to control a read operation on the memory cells;

a page buffer circuit configured to sense hard decision data and a plurality of soft decision data from each of a plurality of selected memory cells in response to the control of the control logic and output the sensed hard decision data and the plurality of soft decision data as a read result; and

a voltage generation circuit configured to generate a plurality of read voltages for reading the hard decision data and the plurality of soft decision data in response to the control of the control logic, wherein

the plurality of soft decision data are sensed between adjacent pieces of threshold voltage distribution, wherein

the plurality of soft decision data included in the read result are encoded into reliability data to be outputted, wherein

the page buffer circuit includes a plurality of page buffers corresponding respectively to the selected memory cells, wherein

each of the page buffers includes a plurality of first type latches to encode the reliability data by values latched in response to values of the plurality of soft decision data being toggled and a second type latch to latch the hard decision data, and wherein

reliability data are encoded in the plurality of first type latches.

<The different feature>

A point that, in the Amended Invention, it is made such that "reliability data" "are expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data", whereas, in the Cited Invention, it is not specified in that manner.

(4) Judgment by the body

Although "soft value 1" and "soft value 2" of the Cited Invention are expressed by two bits, and there is no explanation regarding the number of bits necessary for expressing "soft value 1 (pre1) to soft value 1 (pre3), soft value 1" (four times of repetition) and "soft value 2 (pre1) to soft value 2 (pre7), soft value 2" (eight times of repetition) of the Cited Invention, it can be understood as constituting data formats repeatedly sensed in read operations as reliability data of two bits as an aspect of "being expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data", and, therefore, it can be said that, also in the Cited Invention, "soft value 1" and "soft value 2" are expressed by a number of bits (two bits) that is smaller than the number of bits necessary for expressing "soft value 1 (pre1) to soft value 1 (pre3), soft value 1" (four sets) and "soft value 2 (pre1) to soft value 2 (pre7), soft value 2" (eight sets).

Furthermore, regarding that "reliability data" of the Amended Invention "are expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data", there is described in [0049] of the description of the present application that "although a data format sensed in the seven-times of repeated read operations is identical with that of FIG. 7, data outputted actually have a predetermined data pattern as shown in FIG. 8. (Omitted) Read data outputted through the page buffer PB can be constituted by 1 bit of hard decision data and 2 bits of reliability data.", and, therefore, when it is understood as an aspect in which data formats sensed by seven-time repeated read operations are expressed in one bits of hard decision data and two bits of reliability data, there is no substantial difference with the

Cited Invention.

Even if another aspect other than that can be understood regarding expressing by the number of bits less than the number of bits necessary for expressing a plurality of soft decision data, since there is described in [0060] of the description of the present application that "reliability data outputted from the page buffer PB in the present invention can have values of '01, 00, 10 and 11'. The degree of reliability of data can be constituted in order of 11 > 01 > 00 > 11", "reliability data" are only expressing four degrees in two bits, and thus there is no particular difficulty in expressing 4 degrees in two bits. In other words, it is a matter that can be done by a person skilled in the art accordingly to make "reliability data" "be expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data".

Accordingly, the different feature is not a particular one.

As examined above, the configuration concerning the different feature is one that could have easily been derived by a person skilled in the art, and the function and effect exerted by the Amended Invention is just function and effect within a range predicted from the function and effect exerted by the above-mentioned Cited Invention, and, thus it cannot be regarded as a particularly distinguishing effect.

Therefore, the Amended Invention could have been easily invented by a person skilled in the art based on the above-mentioned Cited Invention, and the appellant should not be granted a patent for this independently at the time of patent application under the provisions of Article 29(2) of the Patent Act.

4 Closing of the decision to decline the Amendment

Since, as has been pointed out in the above-mentioned "4 Judgment on independent requirements for patentability", the appellant should not be granted a patent independently for the invention according to claim 1 after amendment at the time of filing of the patent application, the amendment violates the provisions of Article 126(7) of the Patent Act as applied mutatis mutandis pursuant to the provisions of Article 17-2(6) of the same Act, and, therefore, it should be dismissed under the provisions of Article 53(1) of the same Act which is applied mutatis mutandis pursuant to the provisions of Article 159(1) of the same Act.

Accordingly, decision has resulted in the above-mentioned decision to decline the Amendment.

No. 3 Regarding the invention of the case

1 The Invention

Since the Amendment dated Jul. 1, 2015 has been dismissed as described above, the invention according to claim 1 before amendment (hereinafter, referred to as the "Invention") corresponding to claim 1 after amendment is as follows, as specified by the matters described in claim 1 of the scope of claims amended by the Amendment dated Sep. 12, 2014.

"A flash memory device comprising:

a memory cell array including a plurality of memory cells;

a control logic configured to control a read operation on the plurality of memory cells;

a page buffer circuit configured to sense hard decision data and a plurality of soft decision data from each of a plurality of selected memory cells in response to the control of the control logic and output the sensed hard decision data and the plurality of soft decision data as a read result; and

a voltage generation circuit configured to generate a plurality of read voltages for reading the hard decision data and the plurality of soft decision data in response to the control of the control logic, wherein

the plurality of soft decision data are sensed between adjacent pieces of threshold voltage distribution."

2 Technical matters described in Cited Documents and the Cited Invention

The Cited Invention cited in the reasons for refusal stated in the examiner's decision is as described in "(2) Cited Document" of "4 Judgment on independent requirements for patentability" in "No. 2 Decision to dismiss amendment for the Amendment dated Jul. 1, 2015".

3. Comparison / Judgment

The Invention is an invention from which: regarding "soft decision data" that is a matter specifying the invention of the Amended Invention examined in "4 Judgment on independent requirements for patentability " of "No. 2 Decision to dismiss amendment for the Amendment dated Jul. 1, 2015", the limitation matter of "the plurality of soft decision data included in the read result are encoded into reliability data to be outputted" has been deleted; and, regarding "page buffer circuit", the limitation matter of "the page buffer circuit includes a plurality of page buffers corresponding

respectively to the selected memory cells, wherein each of the page buffers includes a plurality of first type latches to encode the reliability data by values latched in response to values of the plurality of soft decision data being toggled and a second type latch to latch the hard decision data, and wherein the reliability data are expressed by a number of bits smaller than a number of bits necessary for expressing the plurality of soft decision data by being encoded in the plurality of first type latches" has been eliminated.

Then, since, as has been described in "(2) Cited Document" to "(4) Judgment by the body" of "4 Judgment on independent requirements for patentability" of the "No. 2 Decision to dismiss amendment for the Amendment dated Jul. 1, 2015", the Amended Invention including all matters specifying the invention of the Invention could have been easily invented by a person skilled in the art based on the Cited Invention, the Invention made by eliminating the above-mentioned specific limitations could have been also easily invented by a person skilled in the art based on the Cited Invention for the similar reason.

No. 4 Closing

As mentioned above, the appellant should not be granted a patent for the invention according to claim 1 of the present application in accordance with the provisions of Article 29(2) of the Patent Act, and, therefore, without examining the inventions according to the other claims, the present application should be rejected.

Therefore, the appeal decision shall be made as described in the conclusion.

Jun. 9, 2016

Chief administrative judge: TSUJIMOTO, Yasutaka
Administrative judge: TAKAGI, Susumu
Administrative judge: SUDA, Katsumi