Appeal decision

Appeal No. 2015-15152

Osaka, Japan
Appellant PANASONIC INTELLECTUAL PROPERTY MANAGEMENT CORPORATION

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The case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2011-126233, entitled "SOLAR CELL MANUFACTURING METHOD" [the application published on December 20, 2012, Japanese Unexamined Patent Application Publication No. 2012-253261, Claims (four claims)] has resulted in the following appeal decision.

Conclusion

The examiner's decision is revoked.

The invention of the present application shall be granted a patent.

Reason

No. 1 History of the procedures

The application was filed on June 6, 2011, a notice of reasons for refusal was issued as of December 26, 2014, a written opinion was submitted as of February 17, 2015, a written amendment was submitted on February 17, 2015, a decision for refusal (hereinafter referred to as "the examiner's decision") was issued on May 22, 2015, and an appeal against the examiner's decision of refusal was requested and a written amendment submitted on August 12, 2015. A notice of reasons for refusal (hereinafter

referred to as "reasons for refusal of the body") was issued by the body on May 13, 2016, a written opinion was submitted on July 5, 2016, and a written amendment was submitted on July 5, 2016.

No. 2 The Invention

The inventions relating to Claims 1-4 of the application are recognized to be specified by the matters described in Claims 1-4 of the scope of claims corrected by the amendment as of July 5, 2016. The invention relating to Claim 1 of the application (hereinafter referred to as "the Invention") is as follows.

"[Claim 1]

A solar cell manufacturing method including the steps of:

forming a first semiconductor layer including an amorphous silicon layer of one conductivity type by deposition on a first principal surface of a semiconductor substrate having the one conductivity type;

forming a second semiconductor layer including an amorphous silicon layer of another conductivity type by deposition on a second principal surface of the semiconductor substrate;

applying hydrogen radical treatment without using ions to at least one of the first and second semiconductor layers;

exposing the semiconductor substrate with the first and second semiconductor layers formed thereon to the atmosphere after the hydrogen radical treatment;

and forming a transparent conductive oxide layer on the semiconductor layer subjected to hydrogen radical treatment without using ions, of the first and second semiconductor layers."

No. 3 Reasons for refusal stated in the examiner's decision

1 Outline of reasons for refusal stated in the examiner's decision

(1) The Invention is an invention described in the following publication distributed in Japan or abroad before the application was filed or an invention available to the public through electric telecommunication lines. The invention falls under Article 29-1(3) of the Patent Act, and thus the appellant should not be granted a patent for the Invention.

(2) The Invention could have been easily made by a person skilled in the art before the application was filed, on the basis of the invention described in the following publication distributed in Japan or abroad before the application was filed or an invention available to the public through electric telecommunication lines, and thus the appellant should not be granted a patent for the Invention in accordance with the

provisions of Article 29-2 of the Patent Act.

Note

Claims 1, 2

1. Japanese Unexamined Patent Application Publication No. 2005-154795 (hereinafter referred to as "Cited document 1")

The description in [0021] or the like in Cited document 1 indicates hydrogen radical treatment without using ions, and thus there is no remarkable difference between the inventions relating to the Claims 1, 2 and the invention described in Cited document 1.

Claims 3-5

1. Japanese Unexamined Patent Application Publication No. 2005-154795 (Cited document 1)

2. Japanese Unexamined Patent Application Publication No. 2004-289058 (hereinafter referred to as "Cited document 2")

A person skilled in the art could have easily conceived of making the inventions relating to Claims 3-5 by applying the technology described in Cited document 1 to the invention described in Cited document 2.

2 Judgment of the reasons for refusal stated in the examiner's decision

(1) Described Matters in Publication

A Cited document 1

(A) The following matters are described in Cited document 1 (Japanese Unexamined Patent Application Publication No. 2005-154795) (The underlines were added by the body)

a "[0013]

The method for introducing hydrogen into the silicon substrate can employ one method of using a hydrogen-containing gas or a hydrogen gas selected from the group consisting of a plasma method, a foaming gas annealing method, and a Cat-CVD method. Hydrogen can be efficiently introduced into the silicon substrate by one of the above methods.

[0014]

In the plasma method, hydrogen is introduced into the silicon substrate by using hydrogen radicals and/or hydrogen ions dissociated by applying a high-frequency voltage to the hydrogen-containing gas or the hydrogen gas.

[0015]

Hydrogen is introduced into a silicon substrate by the plasma method as follows, for example: disposing a silicon substrate on one of two electrodes facing each other in a reaction container in vacuum atmosphere, and supplying a hydrogen-containing gas or a hydrogen gas into the reaction container; applying a high-frequency voltage between the electrodes by use of a high-frequency power source, to dissociate hydrogen in the reaction container, thereby generating hydrogen radicals and/or hydrogen ions; and introducing hydrogen into the silicon substrate by using the generated hydrogen radicals and/or hydrogen ions terminating dangling bonds present on a surface of the silicon substrate and/or in a grain boundary.

[0016]

In the plasma method, hydrogen is dissociated preferably by supplying a hydrogen gas after heating the silicon substrate up to about 400°C in the reaction chamber in a vacuum atmosphere of several milli-Torr to several Torr, and applying a voltage between the electrodes with the high-frequency power source.

[0017]

In the foaming gas annealing method, hydrogen is introduced into the silicon substrate by using hydrogen radicals and/or hydrogen ions dissociated by heating a hydrogen-containing gas or a hydrogen gas existing in the reaction chamber.

[0018]

Hydrogen is introduced into a silicon substrate by the foaming gas annealing method as follows, for example: disposing the silicon substrate in a reaction chamber in an atmospheric atmosphere made of quartz; supplying a hydrogen-containing gas or a hydrogen gas into the reaction chamber; heating the silicone substrate and the inside of the reaction chamber up to about 400°C; and causing hydrogen radicals and/or hydrogen ions generated by dissociating hydrogen in the reaction chamber to terminate dangling bonds present on the surface of the silicone substrate and/or in a grain boundary.

[0019]

In the foaming gas annealing method, the inside of the reaction chamber is in an atmospheric atmosphere in forming a thin film, and thus hydrogen can be introduced into the silicon substrate more inexpensively than the plasma method or Cat-CVD method. There is no plasma damage to the silicon substrate, as well.

[0020]

In the Cat-CVD method, hydrogen is introduced into a silicon substrate by using hydrogen radicals and/or hydrogen ions dissociated by bringing a hydrogen-containing gas or a hydrogen gas into contact with a heated catalyst.

(See Appl. Phys. Lett. 71 (15), 13, pp. 2169-2171 (1997))

[0021]

Hydrogen is introduced into a silicon substrate by the Cat-CVD method as follows, for example: heating a tungsten wire, serving as a catalyst, disposed in the reaction chamber up to 1700-2000°C; spraying a hydrogen-containing gas or a hydrogen gas onto the heated tungsten wire, to dissociate hydrogen in the reaction chamber into hydrogen radicals and/or hydrogen ions; bringing the hydrogen radicals and/or hydrogen ions into contact with the silicon substrate heated up to about 200-400°C; and causing the hydrogen radicals and/or hydrogen ions to terminate dangling bonds present on the surface of the silicon substrate and/or a grain boundary."

b "[0034]

(Solar cell)

FIG. 2 shows a flow chart of one preferable example of a solar cell manufacturing method. In step 1, a texture structure is formed on a surface of a p-type polycrystalline silicon substrate in order to remove a damage layer formed due to cutting the substrate and to increase antireflection effect. The texture structure is formed by dry etching, such as reactive ion etching, by wet etching using alkali solution, or mechanically.

[0035]

In step 2, an n-type impurity, such as phosphorus, is diffused on the p-type polycrystalline silicon substrate, to form a p-n junction. The p-n junction can be formed by heating the silicon substrate after applying the solution containing an n-type impurity, such as phosphorus, onto the surface of the p-type polycrystalline silicon substrate.

[0036]

In step 3, hydrogen is introduced into the silicon substrate with a p-n junction formed therein. Hydrogen is introduced into the silicon substrate by, for example, the plasma method, foaming gas annealing method, or Cat-CVD method, as described above.

[0037]

In step 4, the silicon substrate is heated by a heater or the like, so as to heat the surface of the silicon substrate in a range of 350 to 500°C.

[0038]

In step 5, a material solution of a thin film is sprayed from a spray nozzle or the like to the surface of the silicon substrate heated in the range of 350-500°C, to form a

thin film. Step 4 of heating the silicon substrate and step 5 of spraying the material solution of the thin film are alternately repeated multiple times.
[0039]

In step 6, a surface electrode and a back electrode are formed on the silicon substrate with the thin film formed thereon. The electrodes can be formed as follows, for example: printing silver paste containing silver powder on a surface of the thin film; printing aluminum paste containing aluminum powder on a back of the silicon substrate; heating the whole of the silicon substrate; and forming a silver surface electrode and an aluminum back electrode. The surface electrode is coated with solder."

(B) Cited document 1 is recognized to describe the following invention (hereinafter referred to as "Cited invention 1"). Paragraph numbers for citations are added for reference.

"The solar cell manufacturing method (paragraph 0034) including:

forming a texture structure on a surface of a p-type polycrystalline silicon substrate (paragraph 0034);

diffusing an n-type impurity, such as phosphorus, on the p-type polycrystalline silicon substrate, to form a p-n junction (paragraph 0035);

introducing hydrogen into the silicon substrate with the p-n junction formed therein by employing one method of using hydrogen radicals and/or hydrogen ions selected from a group comprising a plasma method, a foaming gas annealing method, and a Cat-CVD method (paragraph 0036, paragraphs 0013-0021);

forming a thin film (paragraph 0038);

and forming a silver surface electrode and aluminum back electrode, on the silicon substrate with the thin film formed thereon (paragraph 0039)."

B Cited document 2

(A) Cited document 2 (Japanese Unexamined Patent Application Publication No. 2004-289058) describes the following matters. (Underlines were added by the body)

a "[0001]

[Technical field related to the Invention]

This invention relates to a method for manufacturing a photovoltaic device, especially for manufacturing a photovoltaic device including an amorphous semiconductor layer formed on a crystalline semiconductor."

b "[0010]
In this case, an acceleration voltage to be applied to an electric field for accelerating hydrogen ion is preferably 1eV to 5keV. Thus, the irradiated hydrogen ions can be prevented from reaching a boundary between the substantially authentic amorphous semiconductor layer and the crystalline semiconductor. Therefore, damage to the boundary between the substantially authentic amorphous semiconductor layer and the crystalline semiconductor due to hydrogen ion irradiation can be prevented."

c "[0016]
(First embodiment)
FIG. 1 is a cross-sectional view of a structure of the photovoltaic device in a first embodiment of the invention. The structure of the photovoltaic device in the first embodiment is described below, with reference to FIG. 1.
[0017]
In the photovoltaic device in the first embodiment, as shown in FIG. 1, an amorphous silicon layer 2, a surface electrode 3 made of ITO (Indium Tin Oxide) having a thickness of about 70-100 nm, and a collector 4 made of silver having a thickness of several tens μm are formed sequentially on a top surface of a hydrotreated n-type monocrystalline silicone substrate 1. The amorphous silicon layer 2 is formed of a substantially authentic i-type amorphous silicon layer 2a having a thickness of about 9-13 nm and formed on the top surface of the n-type monocrystalline silicon substrate 1, and a boron (B)-doped p-type amorphous silicon layer 2b having a thickness of about 2-5 nm and formed on the i-type amorphous silicon layer 2a.
[0018]
In the first embodiment, the i-type amorphous silicon layer 2a on an incident side is formed so as to have a peak of hydrogen concentration in the i-type amorphous silicon layer 2a. The n-type monocrystalline silicon substrate 1 is one example of the 'crystalline semiconductor' in the invention. The i-type amorphous silicon layer 2a is one example of the 'amorphous semiconductor layer' in the invention.
[0019]
On the back of the n-type monocrystalline silicon substrate 1, sequentially from the side closer to the back of the n-type monocrystalline silicon substrate 1, there are formed an amorphous silicon layer 12, a back electrode 13 made of ITO having a thickness of about 70-100 nm, and a collector 14 made of silver having a thickness of several tens μm. The amorphous silicon layer 12 is formed of a substantially authentic i-type

amorphous silicon layer 12a having a thickness of about 9-13 nm and formed on the back of the n-type amorphous monocrystalline silicon substrate 1, and a phosphorus (P)-doped n-type amorphous silicon layer 12b having a thickness of about 10-20 nm and formed on the back of the i-type amorphous silicon layer 12a. The i-type amorphous silicon layer 12a, the n-type amorphous silicon layer 12b, and the back electrode 13 form a so-called BSF (Back Surface Field) structure.

[0020]

A manufacturing process of the photovoltaic device in the first embodiment is described below, with reference to FIG. 1. As shown in FIG. 1, after a cleaned n-type monocrystalline silicon substrate 1 is disposed in a vacuum chamber (not shown), the n-type monocrystalline silicon substrate 1 is heated under a temperature condition of about 200°C or lower, and moisture on the surface of the n-type monocrystalline silicon substrate 1 is removed as much as possible. Thus, a defect to be caused by combining oxygen in the moisture on the surface of the n-type monocrystalline silicon substrate 1 with silicon can be prevented.

[0021]

The back of the n-type monocrystalline silicon substrate 1 is subjected to hydrogen treatment, by introducing hydrogen (H_2) gas, with a temperature of the substrate held at about 170°C, and executing plasma discharge. The back of the n-type monocrystalline silicon substrate 1 is cleaned, and hydrogen atoms are adsorbed near the back of the n-type monocrystalline silicon substrate 1. The adsorbed hydrogen atoms deactivate a defect on the back of the n-type monocrystalline silicon substrate 1.

[0022]

By using the RF plasma CVD method, under the condition of a substrate temperature of about 170°C, a hydrogen (H_2)-gas flow rate of 0-about 1000 sccm, a silane (SiH_4)-gas flow rate of about 40 sccm, a pressure of about 40Pa, and RF power density of about 8.33m W/cm^2, the i-type amorphous silicon layer 12a having a thickness of about 9-13 nm is formed on the back of the n-type monocrystalline silicon substrate 1.

[0023]

By using the RF plasma CVD method, under the condition of a substrate temperature of about 170°C, a hydrogen (H_2)-gas flow rate of 0-about 1000 sccm, a silane (SiH_4)-gas flow rate of about 40 sccm, a phosphine (PH_3)/H_2 (concentration of PH_3 with respect to H_2 is about 1%) gas flow rate of about 40 sccm, a pressure of about 40Pa, and RF power density of about 8.33mW/cm^2, the phosphorus (P)-doped n-type amorphous silicon layer 12b having a thickness of about 10-20 nm is formed on the back of the i-type amorphous silicon layer 12a."

d "[0025]

Hydrogen treatment similar to the hydrogen treatment applied to the back of the n-type monocrystalline silicon substrate 1 is applied also to the top surface of the n-type monocrystalline silicon substrate 1. After that, the i-type amorphous silicon layer 2a having a thickness of about 9-13 nm is formed on the top surface of the n-type monocrystalline silicon substrate 1 by using the RF plasma CVD method. In the first embodiment, the condition of forming the i-type amorphous silicon layer 2a is changed in the following order: (1) low-hydrogen condition, (2) high-hydrogen condition, and (3) low-hydrogen condition. The hydrogen concentration peak is formed in the i-type amorphous silicon layer 2a. The high-hydrogen condition enables a large number of hydrogen atoms to be introduced into the i-type amorphous silicon layer 2a. The low-hydrogen condition enables introduction of a smaller number of hydrogen atoms than the high-hydrogen condition into the i-type amorphous silicon layer 2a. Specifically, the high-hydrogen condition specifies a substrate temperature of about 170°C, a hydrogen (H_2)-gas flow rate of 0-about 1000 sccm, a silane (SiH_4)-gas flow rate of about 40 sccm, a pressure of about 40 Pa, and RF power density of about 8.33-80 mW/cm^2. The low-hydrogen condition specifies a substrate temperature of about 170°C, a hydrogen (H_2)-gas flow rate of 0 sccm, a silane (SiH_4)-gas flow rate of about 40 sccm, a pressure of about 40Pa, and RF power density of about 8.33 mW/cm^2."

e "[0027]

After forming the i-type amorphous silicon layer 2a as described above, in the first embodiment, hydrogen ions (H^+) accelerated by an electric field with an acceleration voltage of about 1eV to about 5keV applied thereto are irradiated on the top surface of the i-type amorphous silicon layer 2a. Then, the i-type amorphous silicon layer 2a is heated up to about 100-250°C. Thus, hydrogen is introduced near a depth of about 2-3 nm from the top surface of the i-type amorphous silicon layer 2a. Another hydrogen concentration peak is formed, in addition to the hydrogen concentration peak formed by the above high-hydrogen condition, at a depth about 2-3 nm from the top surface (a boundary between the i-type amorphous silicon layer 2a and the p-type amorphous silicon layer 2b) of the i-type amorphous silicon layer 2a."

f "[0029]

Subsequently, by using the RF plasma CVD method, under the condition of a substrate temperature of about 170°C, a hydrogen (H_2)-gas flow rate of 0-about 1000 sccm, a

silane (SiH_4)-gas flow rate of about 40 sccm, a diborane (B_2H_6)/H_2 (concentration of B_2H_6 gas with respect to H_2 is about 2%) gas flow rate of about 40sccm, a pressure of about 40Pa, and RF power density of about 8.33mW/cm^2, the boron (B)-doped p-type amorphous silicon layer 2b having a thickness of about 2-5 nm is formed on the i-type amorphous silicon layer 2a."

(B) Cited document 2 is recognized to describe the following invention (hereinafter referred to as "Cited invention 2"). Paragraph numbers for citations are added for reference.

"The method for manufacturing a photovoltaic device (paragraph 0001) includes:

forming a substantially authentic i-type amorphous silicon layer 2a on a top surface of an n-type monocrystalline silicon substrate 1, and forming a p-type amorphous silicon layer 2b on the i-type amorphous silicon layer 2a (paragraph 0017);

forming a substantially authentic i-type amorphous silicon layer 12a on the back surface of the n-type monocrystalline silicon substrate 1, and forming an n-type amorphous silicon layer 12b on the back of the i-type amorphous silicon layer 12a (paragraph 0019);

applying hydrogen treatment to the back of the n-type monocrystalline silicon substrate 1 (paragraph 0021);

forming the i-type amorphous silicon layer 12a so as to contain hydrogen (paragraph 0022);

forming the n-type amorphous silicon layer 12b so as to contain hydrogen (paragraph 0023);

applying hydrogen treatment to the top surface of the n-type monocrystalline silicon substrate 1 (paragraph 0025);

forming the i-type amorphous silicon layer 2a so as to contain hydrogen (paragraph 0025);

irradiating hydrogen ions onto the top surface of the i-type amorphous silicon layer 2a after forming the i-type amorphous silicon layer 2a (paragraph 0027);

and forming the p-type amorphous silicon layer 2b so as to contain hydrogen (paragraph 0029)."

(2) Comparison

A Comparing the Invention and Cited invention 1, "p-type" and "n-type" in the Cited invention correspond to "one conductivity type" and "another conductivity type" in the

Invention, respectively.
The Invention and the Cited invention 1 are in correspondence in the following points, "the solar cell manufacturing method including the steps of:

forming a semiconductor layer of one conductivity type on a first principal surface;

forming a second semiconductor layer of another conductivity type on a second principal surface;

and applying hydrogen radical treatment to at least one of the first and second semiconductor layers."

B The Invention and Cited invention 1 are different from each other in the following points.

(A) Different feature 1

The steps of forming a semiconductor layer of one conductivity type on a first principal surface and forming a semiconductor layer of another conductivity type on a second principal surface correspond to, in the Invention, "a step of forming a first semiconductor layer including an amorphous silicon layer of one conductivity type by deposition on a first principal surface of a semiconductor substrate having the one conductivity type, and a step of forming a second semiconductor layer including an amorphous silicon layer of another conductivity type by deposition on a second principal surface of the semiconductor substrate", while in Cited invention 1, it corresponds to the step where "an n-type impurity, such as phosphorus, is diffused on the p-type polycrystalline silicon substrate, to form a p-n junction".

(B) Different feature 2

Regarding the step of applying hydrogen radical treatment, the Invention describes "a step of applying hydrogen radical treatment without using ions", while Cited invention 1 describes "a step of applying hydrogen radical treatment" but does not specify that the hydrogen radical treatment does not use ions.

(C) Different feature 3

The Invention includes "a step of exposing the semiconductor substrate with the first and second semiconductor layers formed thereon to the atmosphere after the hydrogen radical treatment, and a step of forming a transparent conductive oxide layer on the semiconductor layer subjected to hydrogen radical treatment without using ions, of the first and second semiconductor layers," while the Cited invention 1 does not

include the steps.

(3) Judgment

The different feature 3 of the different features 1-3 is examined below.

The "step of applying the hydrogen radical treatment" in the configuration relating to the different feature 3 indicates "a step of applying hydrogen radical treatment without using ions to at least one of the first and second semiconductor layers". Thus, the configuration relating to the different feature 3 is considered to include "a step of exposing the semiconductor substrate with the first and second semiconductor layers formed thereon to the atmosphere, and a step of forming a transparent conductive oxide layer on the semiconductor layer subjected to hydrogen radical treatment without using ions, of the first and second semiconductor layers" after "a step of applying hydrogen radical treatment without using ions to at least one of the first and second semiconductor layers".

The Cited document 2 describes Cited invention 2. The Cited invention 2 does not include the configuration relating to the different feature 3.

The Invention including the configuration relating to the different feature 3 exhibits a prominent effect described in [0030] of the Specification, "after forming the semiconductor layers 11, 13, hydrogen radical treatment is applied without using ions before exposing each of the semiconductor layers 11, 13 to the atmosphere. Thus, adhesion between the semiconductor layers 11, 13 and TCO layers 15, 16 can be improved".

The above different feature 3 could not easily be conceived by a person skilled in the art on the basis of the Cited invention 1 and 2.

The Invention is different from the Cited invention 1 in the point of the different feature 3 at least, and it cannot be said that the Invention could be easily conceived. Thus, the Invention cannot be identified as Cited invention 1, and could not easily be conceived by a person skilled in the art on the basis of the Cited inventions 1 and 2.

(4) Summary

As described above, it cannot be said that the Invention is identified as Cited invention 1 and that the invention could be easily made by a person skilled in the art according to Cited inventions 1 and 2.

The inventions relating to Claims 2-4 include all of the matters specifying the

invention of the Invention, and are limited inventions. The inventions cannot be identified as Cited invention 1, as in the case of the Invention, and could not be easily made by a person skilled in the art on the basis of Cited inventions 1 and 2.

Therefore, the application cannot be refused due to the reasons for refusal of the examiner's decision.

No. 4 Reasons for refusal of the body

1 Outline of the reasons for refusal of the body

(1) (Inventive step)

The Invention could be provided easily by a person ordinarily skilled in the art according to an invention described in a publication distributed in Japan and abroad prior to the filing date of the present application or an invention available to the public through electric telecommunication lines, and thus, the appellant should not be granted a patent for the Invention in accordance with the provisions of Article 29-2 of the Patent Act.

Note

<Cited publications>

Japanese Unexamined Patent Application Publication No. 2004-289058 (Cited document 2)

International Publication No. 2010/050363 (hereinafter referred to as "Cited document 3")

The inventions relating to Claims 1-4 could be easily made by a person skilled in the art according to the invention (Cited invention 2) described in Cited document 2, the matters described in Cited document 3, and well-known arts.

(2) (Ministerial Ordinance requirement)

The description of the detailed description of the invention does not meet the requirement stipulated in Article 36-4(1) of the Patent Act in the following points.

Note

Claim 5 describes "a step of forming a transparent conductive oxide layer on at least one of the first and second conductive layers". Claim 1 cited by Claim 5 describes "a step of applying hydrogen radical treatment without using ions to at least one of the first and second semiconductor layers". There can be a semiconductor layer which has not been subjected to hydrogen radical treatment without using ions. Thus,

the invention relating to Claim 5 includes forming a transparent conductive oxide layer only on a semiconductor layer which has not been subjected to hydrogen radical treatment without using ions. However, technical significance cannot be found in forming the transparent conductive oxide layer only on a semiconductor layer which has not been subjected to hydrogen radical treatment without using ions.

Therefore, the detailed description of the invention has not been described in accordance with the applicable ordinance of the Ministry of Economy, Trade and Industry, on the invention relating to Claim 5.

2 Judgment on the reasons for refusal of the body
(1) Reasons for refusal of the body (inventive step)
A Described Matters in publication
(A) Cited document 2

Cited document 2 is the same publication as "Cited document 2" in the reasons for refusal stated in the examiner's decision. See "B Cited document 2" in "(1) Matters described in Publication" of "2 Judgment of the reasons for refusal stated in the examiner's decision" in "No. 3 Reasons for refusal stated in the examiner's decision" for the matters described in Cited document 2 and Cited invention 2.

(B) Cited document 3

Cited document 3 (International Publication No. 2010-050363) describes the following matters. (Underlines are added by the body.)
"[0058]

As described above, the radical generation chamber 8 and the film forming chamber 4 are connected to each other via the openable and closable shutter 9 on which a plurality of holes are provided. Hydrogen radicals are introduced into the film forming chamber 4 through the holes of the shutter 9. The hydrogen ions 42 generated in the radical generation chamber 8 have positive electric charges, and the shutter 9 is applied with a negative-direct-current bias voltage by the wiring 41 for applying a bias voltage. Therefore, substantially the whole of the hydrogen ions 42 generated in the radical generation chamber 8 are adsorbed and trapped by a coulomb force by the shutter 9 that is applied with a negative-direct-current bias voltage as shown in FIG. 14, and the hydrogen ions 42 cannot enter the film forming chamber 4. As a result, mixing of the hydrogen ions 42 into the film forming chamber 4 is suppressed, and ion damage to the microcrystalline silicon film 3 by the hydrogen ions 42 can be suppressed and prevented."

"[0062]

As described above, according to the manufacturing device of a microcrystalline silicon film according to the second embodiment, the shutter 9 can trap the hydrogen ions 42 generated by the radical generation chamber 8 and prevent the mixing of the hydrogen ions 42 into the film forming chamber 4, and can suppress ion damage on the microcrystalline silicon film 3 by the hydrogen ions 42, by applying a negative-direct-current bias voltage to the shutter 9. When an electric-power generation layer (I-type microcrystalline semiconductor layer) is manufactured by using the manufacturing device of a microcrystalline silicon film according to the second embodiment, a thin-film solar cell having higher power-generation efficiency can be manufactured.

B Comparison

Comparing the Invention and Cited invention 2, the "n-type monocrystalline silicone substrate 1", "n-type amorphous silicon layer 12b", "p-type amorphous silicon layer 2b", and the "method for manufacturing a photovoltaic device" in the Cited invention 2 correspond to the "semiconductor substrate having one conductivity type", "amorphous silicon layer of one conductivity type", "amorphous silicon layer of another conductivity type", and the "solar cell manufacturing method" in the Invention, respectively.

The "top surface of the n-type monocrystalline silicon substrate 1" and "the back of the n-type monocrystalline silicon substrate 1" in the Cited invention 2 correspond to the "first principal surface of a semiconductor substrate" and "second principal surface of the semiconductor substrate", respectively.

In light of the above correspondence, the Invention and the Cited invention 2 are in correspondence in the following points,

"a solar cell manufacturing method including the steps of:

forming a first semiconductor layer including an amorphous silicon layer of one conductivity type, on a first principal surface of a semiconductor substrate having the one conductivity type;

and forming a second semiconductor layer including an amorphous silicon layer of another conductivity type, on a second principal surface of the semiconductor substrate", and are different from each other in the following points.

(Different feature A)

The Invention forms an amorphous silicon layer of one conductivity type and an amorphous silicon layer of another conductivity type by deposition, while Cited invention 2 does not specify the deposition.

(Different feature B)

The Invention includes a step of applying hydrogen radical treatment without using ions to at least one of the first and second semiconductor layers, while the Cited invention 2 forms an n-type amorphous silicon layer 12b and a p-type amorphous silicon layer 2b so as to contain hydrogen, and does not specify applying hydrogen radical treatment without using ions.

(Different feature C)

The Invention includes "a step of exposing the semiconductor substrate with the first and second semiconductor layers formed thereon to the atmosphere after the hydrogen radical treatment, and a step of forming a transparent conductive oxide layer on the semiconductor layer subjected to hydrogen radical treatment without using ions, of the first and second semiconductor layers", while the Cited invention 2 does not specify the above steps.

C Judgment

The above different features are examined below.

(A) Different feature A

The method of forming an amorphous silicon layer by deposition is well-known art without citing an example. Thus, a person skilled in the art could easily conceive of forming the "p-type amorphous silicon layer 2b" and the "n-type amorphous silicon layer 12b" in the Cited invention 2 "by deposition" in the configuration relating to the different feature A.

(B) Different feature B

The Cited invention 2 introduces hydrogen in forming the "n-type amorphous silicon layer 12b" and the "p-type amorphous silicon layer 2b". A person skilled in the art can select whether to introduce hydrogen at the same time as forming the layers or after forming the layers. As described in Cited document 3 (especially, see paragraphs 0058 and 0062), a person skilled in the art knows of trapping hydrogen ions without damage in introducing hydrogen, and introducing hydrogen radical selectively. Thus, a person skilled in the art could easily conceived of forming the n-type amorphous

silicon layer 12b and the p-type amorphous silicon layer 2b containing hydrogen in the Cited invention 2, as described in the Cited document 3, after forming the layers, by trapping hydrogen ions to introduce hydrogen radical selectively, or applying hydrogen radical treatment without using ions.

(C) Different feature C

The "step of applying the hydrogen radical treatment" in the configuration relating to the different feature C is identified as the "step of applying hydrogen radical treatment without using ions to at least one of the first and second semiconductor layers". The configuration relating to the different feature 3 is considered to include "the steps of exposing the semiconductor substrate with the first and second semiconductor layers formed thereon to the atmosphere, and forming a transparent conductive oxide layer on the semiconductor layer subjected to hydrogen radical treatment without using ions, of the first and second semiconductor layers" after "the step of applying hydrogen radical treatment without using ions to at least one of the first and second semiconductor layers".

The steps are well-known, but the combination of the steps in this order is not described in Cited document 2 or Cited document 3. There is no evidence for well-known arts, as well.

The Invention including the configuration relating to the different feature C exhibits a prominent effect described in [0030] of the Specification, "after forming the semiconductor layers 11, 13, hydrogen radical treatment is applied without using ions before exposing each of the semiconductor layers 11, 13 to the atmosphere. Thus, adhesion between the semiconductor layers 11, 13 and TCO layers 15, 16 can be improved".

Therefore, it cannot be said that the configuration relating to the different feature C could be easily conceived by a person skilled in the art according to Cited invention 2, the matters described in Cited document 3, and well-known arts.

D Summary

It cannot be said that the Invention could be easily made by a person skilled in the art according to Cited Invention 2, the matters described in Cited document 3, and well-known arts, due to the different feature C.

The inventions relating to Claims 2-4 include all of the matters specifying the invention of the Invention, and are limited inventions. As with the Invention, the inventions could not be easily made by a person skilled in the art according to Cited

invention 2, the matters described in Cited document 3, and well-known arts.

Therefore, the application cannot be refused due to the reasons for refusal of the body on the inventive step notified by the body.

(2) Reasons for refusal of the body (Ministerial Ordinance requirement)

The scope of claims of the application is amended as of July 5, 2016, to add Claim 5 citing Claim 1 before correction, as new Claim 1. The description, "the step of forming a transparent conductive oxide layer on at least one of the first and second semiconductor layers" is corrected to the description, "the step of forming a transparent conductive oxide layer on the semiconductor layer subjected to hydrogen radical treatment without using ions, of the first and second semiconductor layers".

The reasons for refusal of the body on the ministerial ordinance requirement were eliminated.

No. 5 Conclusion

As described above, the application cannot be refused due to the reasons for refusal stated in the examiner's decision. No other reasons for refusal are found.

Therefore, the appeal decision shall be made as described in the conclusion.

August 15, 2016

Chief administrative judge: ITO, Masaya
Administrative judge: MORI, Ryosuke
Administrative judge: MATSUKAWA, Naoki