Advisory opinion

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The case of the advisory opinion on the technical scope of a patent invention for Japanese Patent No. 5726980 between the parties above is stated and concluded as follows.

Conclusion

The "semiconductor device" indicated in the Drawings and explanatory document of Article A falls within the technical scope of the invention in Patent No. 5726980.

Reason

No. 1. Object of the demand

An advisory opinion that the Solid State Drive indicated in the explanatory document of the Article A falls within the technical scope of the patent invention described in Claims 1 and 6 of Patent No. 5726980 is demanded.

No. 2. The Patent invention

The Patent invention is as described in Claims 1 and 6 in the scope of claims, as

viewed from the specification and description of the drawings. The constituent components in the Patent invention will be separately described as follows.

1. Configuration of the Patent invention
(Claim 1)
N. A semiconductor device including:
A. first to n-th nonvolatile semiconductor memories (n is an integer of 2 or more);
B. (n+1)-th to 2n-th nonvolatile semiconductor memories;
C. first to n-th resistive elements;
D. a controller for controlling the first to 2n-th nonvolatile semiconductor memories;
E. first to n-th signal lines for connecting the controller to each of the first to n-th resistive elements;
F. (n+1)-th to 2n-th signal lines for connecting the first to n-th resistive elements to the first to n-th nonvolatile semiconductor memories, respectively;
G. (2n+1)-th to 3n-th signal lines branched from the (n+1)-th to 2n-th signal lines, and connected to the (n+1)-th to 2n-th nonvolatile semiconductor memories, respectively; and
H. a substrate,
I. the substrate including
J. a front surface layer with a wiring pattern formed on a front surface of the substrate, and having the first to n-th nonvolatile semiconductor memories, the first to n-th resistive elements, and the controller mounted thereon,
K. a rear surface layer with a wiring pattern formed on a rear surface of the substrate, and having the (n+1)-th to 2n-th nonvolatile semiconductor memories mounted thereon,
L. and a connector for connecting to an external device,
M. and configured so that the first to n-th nonvolatile semiconductor memories and the (n+1)-th to 2n-th nonvolatile semiconductor memories are arranged symmetrically with respect to the substrate.
(Claim 6)
O. The semiconductor device described in any of Claims 1 to 5, and including an internal wiring layer with a wiring pattern arranged between the front surface layer and the rear surface layer, and configured so that the (2n+1)-th to 3n-th signal lines have portions passing through the internal wiring layer.
(The symbols A to O are used for separate description. The components separately described above are referred to as "Constituent component A," or the like, below with the symbols.)

2. Object of the Patent invention

According to the description of the specification, the object of the Patent invention is as follows.

"[0003]

The above semiconductor devices may have restriction on the shape and size of the substrate in accordance with the use environment thereof, specifications, etc. There is a need to prevent degradation of performance characteristics, while arranging nonvolatile semiconductor storage elements in accordance with the shape and size of the substrate.

[Prior art documents]

[Patent literature]

[0004]

[Patent document 1] Japanese Unexamined Patent Application Publication No. 2010-79445

[Summary of the invention]

[Problem to be solved by the invention]

[0005]

One embodiment of the invention has an object to provide a semiconductor device which can prevent degradation of performance characteristics, while arranging nonvolatile semiconductor elements and so on in accordance with the restrictions on the size and shape of a substrate."

No. 3. Article A

1. Specifications of Article A

The following are described on p. 2 of the explanatory document of Article A which was submitted together with the advisory opinion request on April 28, 2016,

"2 Description of Article A

(1) The Article A includes an aluminum housing of about 100 mm wide and 70 mm long. The characters "Solid State Drive" are printed on the front surface of the housing. (FIG. 1)

A sticker with the name of the model "TS512GSSD370" printed thereon is pasted on the rear surface (FIG. 2).

According to the product sheet of SSD370 series (Evidence A No. 2, p. 13), "TS512GSSD370" means an SSD manufactured by Transcend with a "TS6500" memory controller (hereinafter referred to as "controller") and a 512GB memory

capacity, using an MLC (Multiple Level Cell) memory system. "TS6500" is a controller manufactured by Transcend (Evidence A No. 3: ‘the SSD employs "TS6500" controller manufactured by Transcend for controlling an ultra-high speed MCL flash chip’). The storage medium is a Synchronous MLC NAND flash memory (Evidence A No. 4). Note that, MLC is a system capable of storing 2-bit data per NAND cell. The SSD370 series are classified into SSD370S series having an aluminum housing (Article A) and SSD370 series having a plastic housing. There are varieties of memory capacity, such as 32GB, 64GB, 128GB, 256GB, and 1TB (Evidence A No. 5)." (Explanatory document of Article A p. 2 l. 1-l. 20)

In light of the cited description, the Article A can be understood to belong to SSD370S series including SSDs of multiple capacities. However, the Article A is considered to be one having the characters "TS512GSSD370" printed on the rear surface of a metal housing, on the basis of the above cited descriptions,
"The Article A includes an aluminum housing of about 100 mm wide and 70 mm long. The characters ‘Solid State Drive’ are printed on the front surface of the housing. (FIG. 1),"

and

"A sticker with the name of the model ‘TS512GSSD370’ printed thereon is pasted on the rear surface (FIG. 2)", and the Article A alleged by the demandant can be specified as "TS512GSSD370S" in SSD370S series, on the basis of the pictures in "Product Image" of "SSD370S" in Evidence A No. 4, the description "TS512GSSD370S 512GB" in "SSD370S (Aluminum) Ordering Information" at the bottom left in Evidence A No. 5, and a package image shown at the right. The above matters have been confirmed with facsimile submitted by the demandant as of December 15, 2016.

The demandee alleges in the written reply to the advisory opinion request as of August 18, 2016 (hereinafter referred to as "written reply"),
"(1) General statement

The Solid State Drive indicated in the explanatory document of Article A (hereinafter referred to as ’Article A’) does not satisfy the constituent component M of the patent invention described in Claim 1 (hereinafter referred to as ‘the Invention 1’) of the scope of claims of Patent No. 5726980 (hereinafter referred to as ‘the Patent’).

Thus, the Article A does not belong to the technical scope of the patent invention described in Claim 6 (hereinafter referred to as ‘the Invention 2’) citing the Invention 1 and Claim 1.

The demandant specifies, in the explanatory document of Article A, the Article A from the model name ‘TS512GSSD370’ printed on the Article A. However, the

Solid State Drive referred by the demandee, ‘TS512GSSD370’ employs multiple kinds of printed circuit boards (PCB). The Article A cannot be specified only by the model name, accordingly.

Thus, the Article A indicated by the demandant in the explanatory document of Article A uses one of multiple kinds of PCBs. The PCB used in this case can be specified (or the Article A can be specified) only with the information printed on an internal printed circuit board. Therefore, the Article A cannot be specified only by the appearance of the product.

We must also add for confirmation that the Article A in the advisory opinion is specified only with the information ‘29-5000 VI. 1 VIC 3C’ printed on an internal PCB (printed at the top right of FIG. 3 (figure below) in the explanatory document of Article A) (specifically, the Article A in the advisory opinion should be limited to the product with 512G 29-5000 VI. 1 VIC 3C in SSD370 series)." (Written reply p. 2, l. 12-p. 3, l. 9)

In response to the allegation, the demandant alleges in the written refutation as of September 21, 2016 (hereinafter referred to as "written refutation")
"(1) Scope of Article A

The demandee alleges that the Solid State Drive treated by the demandee ‘TS512GSSD370’ employs one printed circuit board (PCB) (one of multiple kinds of PCBs), that the type thereof can be specified with the information ‘29-5000 VI. 1 VIC 3C’ printed at the top left of FIG. 5 in the explanatory document of Article A, and that the Article A in the advisory opinion should be limited to the product with 512G 29-5000 VI. 1 VIC 3C in SSD370 series (p. 2, the 7th line from the bottom to p. 3, l. 15).

However, the demandee has never proven that the PCB of ‘TS512GSSD370’ has multiple kinds, or that the type of the PCB can be specified with the information ‘29-5000 VI. 1 VIC 3C’ printed at the top right in FIG. 3 (figure below) of the explanatory document of Article A. At least, there is no description that there are multiple kinds of PCBs, in the product sheet of SSD370 series (Evidence A No. 2).

Thus, the demandee's allegation is not based on the evidence and is groundless." (Written refutation p. 2, l. 16-p. 3, l. 6)

Considering both the above allegations,

"The information ‘29-5000 V1. 1 VIC 3C’ printed on an internal PCB (printed at the top right of FIG. 3 (figure below) in the explanatory document of Article A)” alleged by the demandee in the written reply cannot be recognized as "information ‘29-

5000 VI. 1 VIC 3C’ printed on an internal printed circuit board" in "FIG. 3 of the explanatory document of Article A" or any of the pictures of the substrate of the Article A attached by the demandant. However, there is no contradiction in accepting that the information "29-5000 VI. 1 VIC 3C" is printed at the top right of FIG. 3 of the explanatory document of Article A.

The demandant does not argue specifically against the matter that "29-5000 VI. 1 VIC 3C" is printed.

Neither party has presented any evidence for the existence of variety of circuit arrangements and configurations in the SSD370 series. The presence of variation remains unclear.

We therefore make an advisory opinion for, as Article A,
"a substrate No. 29-5000 VI. 1 VIC 3C" in “TS512GSSD370S".

2. Configuration of Article A

In light of the contents described in the explanatory document of Article A and the contents described in Evidences A No.2-7, Article A is recognized to have the following constituents:

N. A semiconductor device including:
A. first to fourth NAND flash memories;
B. fifth to eighth NAND flash memories;
C. first to fourth resistive elements;
D. a controller for controlling the first to eighth NAND flash memories;
E. first to fourth signal lines for connecting the controller to each of the first to fourth resistive elements;
F. fifth to eighth signal lines for connecting the first to fourth resistive elements to the first to fourth NAND flash memories, respectively;
G. ninth to 12th signal lines branched from the fifth to eighth signal lines, and connected to the fifth to eighth NAND flash memories, respectively; and
H. a wiring substrate formed of first to eighth layers including a front surface layer and a rear surface layer,
I. the wiring substrate including
J. the front surface layer with a wiring pattern formed on a front surface of the substrate, including the first to fourth signal lines, and having the first to fourth NAND flash memories, the first to fourth resistive elements, and the controller mounted thereon,
K. the rear surface layer with a wiring pattern formed on a rear surface of the substrate,

including the ninth to 12th signal lines, and having the fifth to eighth NAND flash memories mounted thereon,
L. and a SATA22 pin connector,
M. and configured so that the first to fourth NAND flash memories mounted on the front surface and the fifth to eighth NAND flash memories mounted on the rear surface are arranged symmetrically with respect to the wiring substrate,
O. the semiconductor device including an internal wiring layer with a wiring pattern arranged between the front surface layer and the rear surface layer and formed of the second to seventh layers, and configured so that the ninth to 12th signal lines have portions passing through the internal wiring layer.

No. 4 Comparison between the Patent invention and Article A
1. Regarding Constituent component A

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "first to fourth NAND flash memories" in the Article A are obviously nonvolatile semiconductor memories, and correspond to the "first to n-th (n is an integer of 2 or more) nonvolatile semiconductor memories" in the Patent invention.

Thus, the configuration A of the Article A satisfies the Constituent component A in the Patent invention.
2. Regarding Constituent component B

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "fifth to eighth NAND flash memories" in the Article A are also nonvolatile semiconductor memories, and correspond to the "(n+1)-th to 2n-th nonvolatile semiconductor memories" in the Patent invention.

Thus, the configuration B of the Article A satisfies the Constituent component B in the Patent invention.
3. Regarding Constituent component C

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "first to fourth resistive elements" in the Article A correspond to the "first to n-th resistive elements" in the Patent invention.

Thus, the configuration C of the Article A satisfies the Constituent component C in the Patent invention.
4. Regarding Constituent component D

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "controller for controlling the first to eighth NAND flash memories" in the Article A corresponds to the "controller for controlling the first to 2n-th nonvolatile semiconductor memories" in the Patent invention.

Thus, the configuration D of the Article A satisfies the Constituent component D in the Patent invention.

5. Regarding Constituent component E

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "first to fourth signal lines for connecting the controller to each of the first to fourth resistive elements" in the Article A correspond to the "first to n-th signal lines for connecting the controller to each of the first to n-th resistive elements" in the Patent invention.

Thus, the configuration E of the Article A satisfies the Constituent component E in the Patent invention.

6. Regarding Constituent component F

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "fifth to eighth signal lines for connecting the first to fourth resistive elements to the first to fourth NAND flash memories, respectively" in the Article A correspond to the "(n+1)-th to 2n-th signal lines for connecting the first to n-th resistive elements to the first to n-th nonvolatile semiconductor memories, respectively" in the Patent invention.

Thus, the configuration F of the Article A satisfies the Constituent component F in the Patent invention.

7. Regarding Constituent component G

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "ninth to 12th signal lines branched from the fifth to eighth signal lines and connected to the fifth to eighth NAND flash memories, respectively" in the Article A correspond to the "(2n+1)-th to 3n-th signal lines branched from the (n+1)-th to 2n-th signal lines and connected to the (n+1)-th to 2n-th nonvolatile semiconductor memories, respectively" in the Patent invention.

Thus, the configuration G of the Article A satisfies the Constituent component G in the Patent invention.

8. Regarding Constituent components H and I

Sufficiency is not disputed about the constituent components between the demandant and the demandee.

The "wiring substrate formed of first to eighth layers including a front surface layer and a rear surface layer" in the Article A and the "wiring substrate" are "substrates," and correspond to the "substrate" in the Patent Invention.

Thus, the configuration H of the Article A satisfies the Constituent component H in the Patent invention. The configuration I of the Article A satisfies the Constituent component I in the Patent invention.

9. Regarding Constituent component J

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "front surface layer with a wiring pattern formed on a front surface of the substrate, and having the first to fourth signal lines, the first to fourth NAND flash memories, the first to fourth resistive elements, and the controller mounted thereon" in the Article A is a front surface of a wiring substrate, and corresponds to the "front surface layer with a wiring pattern formed on a surface of the substrate, and having the first to n-th nonvolatile semiconductor memories, the first to n-th resistive elements, and the controller mounted thereon" in the Patent invention.

Thus, the configuration J of the Article A satisfies the Constituent component J in the Patent invention.

10. Regarding Constituent component K

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "rear surface layer with a wiring pattern formed on a rear surface of the substrate, including the ninth to 12th signal lines, and having the fifth to eighth NAND flash memories mounted thereon" in the Article A corresponds to the "rear surface layer with a wiring pattern formed on a rear surface of the substrate, and having the (n+1)-th to 2n-th nonvolatile semiconductor memories mounted thereon" in the Patent invention.

Thus, the configuration K of the Article A satisfies the Constituent component K in the Patent invention.

11. Regarding Constituent component L

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "SATA22 pin connector" in the Article A is obviously a "connector" for connecting to an external device, and corresponds to the "connector for connecting to an

external device" in the Patent invention.

Thus, the configuration L of the Article A satisfies the Constituent component L in the Patent invention.

12. Regarding Constituent component M

Considering a technical meaning of the Constituent component M in the Patent invention, the Patent specification includes descriptions about "symmetry" as follows.

"[0038]
In this modified example 1, the NAND memories 10 are mounted also on the rear surface layer of the substrate 8, and the semiconductor device 100 includes eight NAND memories 10. The NAND memories 10 mounted on the rear surface layer of the substrate 8 are arranged in positions symmetrical to the NAND memories 10 mounted on the surface layer of the substrate 8.
[0039]
The resistive elements 12 are not mounted on the rear surface layer of the substrate 8, but are mounted only on the front surface layer. The wires for connecting the resistive elements 12 to the NAND memories 10 are routed in an inner layer of the substrate 8 to be branched by via holes 24, and are drawn out to the rear surface layer L8 as well as the front surface layer L1 of the substrate 8. The NAND memories 10 arranged on the front surface layer are connected to the wires drawn out to the front surface layer L1, while the NAND memories 10 arranged on the rear surface layer are connected to the wires drawn out to the rear surface layer L8. Thus, two NAND memories 10 are connected to one resistive element 12.
[0040]
As described above, the NAND memories 10 are mounted on both surfaces of the substrate 8, thereby increasing memory capacity of the semiconductor device 100. Multiple (two in the modified example) NAND memories 10 can be connected to each resistive element 12 by branching the wire line in the middle of it. The semiconductor device 100 can be equipped with NAND memories 10 with channels greater in number than those of a drive control circuit 4. In this modified example, eight NAND memories can be arranged in the drive control circuit 4 which has four channels. Each of the NAND memories determines whether or not to operate, in accordance with active state of CEs (chip enable) of the NAND memories."

"[0045]
FIG. 12 is a bottom view showing a schematic configuration of a semiconductor device

102 relating to the modified example 1 of a second embodiment. FIG. 13 is a sectional view along a line B-B shown in FIG. 12. In the modified example 1, as with the modified example 1 of a first embodiment, NAND memories 10 are arranged in positions on a rear surface layer of the substrate 8, which are symmetrical to NAND memories 10 arranged on a front surface layer, thereby increasing memory capacity of the semiconductor device 102.

[0046]

When the NAND memories 10 are arranged in positions symmetrical to the NAND memories 10 arranged on the front surface layer of the substrate 8, the NAND memories 10 are arranged close to one long side on the rear surface layer of the substrate 8, thereby reducing the height of the semiconductor device 102 in the region T."

"[0054]

FIG. 16 is a bottom view showing a schematic configuration of a semiconductor device relating to the modified example 1 of a third embodiment. In the modified example 1, as with the modified example 1 of the first embodiment, NAND memories 10 are arranged in positions on a rear surface layer of the substrate 8, which are symmetrical to NAND memories 10 arranged on a front surface layer, thereby increasing memory capacity of a semiconductor device 103.

[0055]

When the NAND memories 10 are arranged in positions symmetrical to the NAND memories 10 arranged on the front surface layer of the substrate 8, the NAND memories 10 are arranged close to one long side on the rear surface layer of the substrate 8, thereby reducing the height of the semiconductor device 103 in a region along the other long side."

"[0061]

FIG. 18 is a bottom view showing a schematic configuration of a semiconductor device relating to the modified example 1 of a fourth embodiment. In the modified example 1, as with the modified example 1 of the first embodiment, NAND memories 10 are arranged in positions on a rear surface layer of the substrate 8, which are symmetrical to NAND memories 10 arranged on a front surface layer, thereby increasing memory capacity of a semiconductor device 104.

[0062]

When the NAND memories 10 are arranged in positions symmetrical to the NAND memories 10 arranged on the front surface layer of the substrate 8, the NAND memories

are arranged close to one long side on the rear surface layer of the substrate 8, thereby reducing the height of the semiconductor device 104 in a region along the other long side." (Underlines added in the descriptions cited from the Patent specification were added for convenience of description by the body.)

According to the descriptions of the Patent specification, "arranged in positions symmetrical to the NAND memories 10 mounted on the front surface layer of the substrate 8," in [0038], "the NAND memories 10 are mounted on both surfaces of the substrate 8, thereby increasing memory capacity of the semiconductor device 100," in [0040], "as with the modified example 1 of a first embodiment, NAND memories 10 are arranged in positions on a rear surface layer of the substrate 8, which are symmetrical to NAND memories 10 arranged on a front surface layer, thereby increasing memory capacity of the semiconductor device 102," in [0045], "In the modified example 1, as with the modified example 1 of the first embodiment, NAND memories 10 are arranged in positions on a rear surface layer of the substrate 8, which are symmetrical to NAND memories 10 arranged on a front surface layer, thereby increasing memory capacity of a semiconductor device 103," in [0054], and "In the modified example 1, as with the modified example 1 of the first embodiment, NAND memories 10 are arranged in positions on a rear surface layer of the substrate 8, which are symmetrical to NAND memories 10 arranged on a front surface layer, thereby increasing memory capacity of a semiconductor device 104," in [0061], the object of the Constituent component M is to "increase memory capacity of a semiconductor device by arranging nonvolatile semiconductor memories on a rear surface layer in positions symmetrical to nonvolatile semiconductor memories arranged on a front surface layer." For this object, it is obvious that the nonvolatile semiconductor memories on the rear surface layer and the nonvolatile semiconductor memories on the front surface layer need not be located in exactly the same positions.

However, the Patent specification does not describe details about a positional relation for "symmetry."

Therefore, in the Patent specification, the term "symmetry" does not mean that the memories are arranged in exactly the same positions on both surfaces of the substrate, and it is sufficient if they are arranged in substantially the same positions.

In the above cited descriptions, other working effects to be generated when the memories are arranged "symmetrical" to each other are described in [0046], [0055], and [0062]. These effects are secondary effects to be generated when the "nonvolatile semiconductor memories" on the rear surface layer are arranged symmetrical to the

arrangement on the front surface layer. It is not recognized that the technical meaning of "symmetrical" should be different from the above.

Considering the configuration of the Article A, it can be recognized that, in the Article A, "the first to fourth NAND flash memories mounted on the front surface" and "the fifth to eighth AND flash memories" are located in substantially the same positions, and it can be said that they are arranged symmetrically with respect to the substrate. The Article A with the arrangement has an effect of doubling memory capacity of the "semiconductor device" or "increasing memory capacity" as with the Patent invention.

Accordingly, the description in the Article A, "the first to fourth NAND flash memories mounted on the front surface and the fifth to eighth NAND flash memories mounted on the rear surface are arranged symmetrically with respect to the wiring substrate" corresponds to the description in the Patent invention, "the first to n-th nonvolatile semiconductor memories and the (n+1)-th to 2n-th nonvolatile semiconductor memories are arranged symmetrically with respect to the substrate."

Thus, the configuration M of the Article A satisfies the Constituent component M in the Patent invention.

13. Regarding Constituent component N

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The "semiconductor device" in the Article A corresponds to the "semiconductor device" in the Patent invention.

Thus, the configuration N of the Article A satisfies the Constituent component N in the Patent invention.

14. Regarding Constituent component O

Sufficiency is not disputed about the constituent component between the demandant and the demandee.

The description in the Article A, "including an internal wiring layer with a wiring pattern arranged between the front surface layer and the rear surface layer and formed of the second to seventh layers, and configured so that the ninth to 12th signal lines have portions passing through the internal wiring layer," corresponds to the description in the Patent invention, "including an internal wiring layer with a wiring pattern arranged between the front surface layer and the rear surface layer, and configured so that the (2n+1)-th to 3n-th signal lines have portions passing through the internal wiring layer."

Thus, the configuration O of the Article A satisfies the Constituent component O in the Patent invention.

15. As discussed in 1. to 14., the configurations A to O satisfy the Constituent components A to O.

No. 5 Demandee's allegation

1. Outline of the demandee's allegation

The demandee alleges as follows in the written reply,

"Evidence B No. 1 (details are described below together with B-2: Note 3) is a blog article on SSD (Solid State Drive) as of February 5, 2009 (‘Note 3’). (The blog article was created by a person irrelevant to the demandee. The article is hereinafter referred to as ‘the known document.’)

The known document includes images of the disassembled SSD and articles about it. According to the posted images (contents of the known document), it can be said that the known document discloses the following configuration of the SSD.

<Configuration of the SSD disclosed in the known document>

The substrate is substantially a rectangle in plain view.

Eight flash memories (nonvolatile semiconductor memories) and one controller are mounted on one side of the substrate.

Eight flash memories (nonvolatile semiconductor memories) are mounted on the other side of the substrate.

A connector is arranged for connecting to an external device.

The flash memories mounted on one side of the substrate and the flash memories mounted on the other side thereof are arranged symmetrically with respect to the substrate. Specifically, the flash memories arranged substantially uniformly in a vertical direction (when two sides orthogonal to a side on which the connector is arranged are defined as an upper side and a lower side, respectively), close to one short side of the substrate (a side opposite the side where the connector is arranged), and not close to either long side of the substrate (a side orthogonal to the side where the connector is arranged), are symmetrical with respect to the substrate.

Furthermore,

resistive elements mounted between the controller and the nonvolatile semiconductor memories arranged on a surface layer of the substrate (the resistive elements are mounted on the surface layer of the substrate) are connected to the controller and the nonvolatile semiconductor memories, respectively, (‘Note 4’) and,

a signal line connecting one nonvolatile semiconductor memory and the resistive element is branched, to be connected to the other nonvolatile semiconductor memory,

(‘Note 5’)
were well-known at the time of filing the original application. In light of the above well-known art, it can be said that the known document describes the Invention 1 as a known art. (Omitted)

According to the fact that the Patent specification describes the following points, the term ‘symmetrical’ described in the Constituent component M should be interpreted, excluding the meaning of ‘symmetrical’ indicated by the known art, as

‘the nonvolatile semiconductor memories mounted on the front surface layer and the rear surface layer of the substrate are arranged, so as to be sufficient to exert the following effects 1 and 2, symmetrical with respect to the substrate, close to one long side of the substrate (one of "upper and lower" sides in a vertical direction, which is the direction of a short side of the substrate in plain view)’

(Omitted)

According to FIG. 5 of the explanatory document of Article A, the nonvolatile semiconductor memories mounted on the front surface layer and the rear surface layer, in the Article A, are arranged symmetrically with respect to the substrate. However, the nonvolatile semiconductor memories are configured to

‘be arranged substantially uniformly in a vertical direction (when two sides orthogonal to a side on which the connector is arranged are defined as an upper side and a lower side, respectively), close to a side of the substrate (opposite the side where the connector is arranged), and not close to a side of the substrate (orthogonal to the side where the connector is arranged).’ (‘Note 7’)

Thus, in light of the fact that the Article A has the same configuration as the known art excluded from the technical scope of the Invention 1, it cannot be said that the Article A is configured, as described in the Constituent component M, so that ‘the nonvolatile semiconductor memories mounted on the front surface layer and the rear surface layer of the substrate are arranged, so as to be sufficient to exert the following effects 1 and 2 ("Note 6"), symmetrical with respect to the substrate, close to one long side of the substrate (one of "upper and lower" sides in a vertical direction, which is the direction of a short side of the substrate in plain view).’

Thus, the Article A does not satisfy the Constituent component M, and does not fall within the technical scope of the Invention 1. (Omitted)" (Excerpts from Written

reply p. 5 l. 13-p. 13 l. 3. Descriptions not relevant to the contents are partially modified.)

2. Judgment by the body for the demandee's allegation

(1) Adoption of Evidence B No. 1 and Evidence B No. 2

Evidence B No. 1 (Livedoor Blog IT/Home appliance "Blog-na MaterialisticA disassembling of SSD manufactured by SILICON POWER" February 5, 2009) submitted by the demandee together with the written reply is a blog article and there are doubts as to the date and contents thereof, while Evidence B No. 2 (an output of a search result as of February 8, 2009 for URL: http://materialistica.livedoor.biz/archive/51427438.html in "INTERNET ARCHIVE" using a service of a web site "WayBackMachine"; August 16, 2016) was prepared by acquiring and storing snapshot of pages of Evidence B No. 1 on February 8, 2009 by Internet Archive which is an organization for acquiring and storing snapshot of web pages, which is not relevant to the organization of the web page for Evidence B No. 1. In light of the purpose of Internet Archive, the stored information is considered to be the same as that acquired. The demandant has not submitted concrete evidence of modification of information in Evidence B No. 2 after February 8, 2009. It cannot be denied that the information in Evidence B No. 2 existed on February 8, 2009, accordingly.

Therefore, we will discuss the matter on the assumption that the "SSD manufactured by SILICON POWER" disclosed in Evidence B No. 2 existed on February 8, 2009.

(2) Whether the Patent invention was known

In order to prove that the Patent invention has been a known art, on the basis of the technology described in Evidence B No. 2 (hereinafter referred to as "the known document"), it must be demonstrated that all of the Constituent components A to O of the Patent invention are described or substantially described in the known document.

We will have a discussion about whether all of the Constituent components A to O of the Patent invention are described in the known art.

According to the known document, there are three images (hereinafter referred to as "Image 1" to "Image 3") in Evidence B No. 2, p. 2/4. There is the following description in four lines below the first image:

"The above image shows a substrate removed from a housing cover at the back side after further disassembling. Eight pieces of ‘K9GA08U0M-PCB0’ are mounted on the

back side of the substrate, as with the front side, and
a controller chip ‘JM602’ manufactured by JMicron is mounted, as well." (Hereinafter referred to as "Cited description 1.")

There are three images different from those in p. 2/4, in p. 3/4 in the known document. There is the following description in 3 lines below the second image: "Accordingly, ‘SP032GBSSD650S25,’ which is an MLC32GB model of the SSD manufactured by SILICON POWER, is a product including 16 MLC flash memories ‘K9GA08U0M-PCB0’ manufactured by SAMSUNG and the controller ‘JM602’ manufactured by JMicron." (Hereinafter referred to as "Cited description 2")

According to the Cited description 1, Image 2, and Image 3, it can be understood that the known document includes "8 pieces of ‘K9GA08U0M-PCB0’ mounted on the front surface side of the substrate and 8 pieces of ‘K9GA08U0M-PCB0’ mounted on the rear surface side of the substrate as with the front surface side, as well as a controller chip ‘JM602’ manufactured by JMicron." According to the Cited description 2, it can be understood that the "K9GA08U0M-PCB0" is an MLC flash memory manufactured by SAMSUNG.

Furthermore, according to the Images 2 and Image 3, the "eight flash memories on the front surface side of the substrate" and the "eight flash memories on the rear surface side of the substrate" are arranged substantially symmetrical to each other.

According to the Images 1 to Image 3, a connector for connecting to another device can be seen at the end of the substrate (a lower end in Image 1, and right ends in Images 2 and Image 3).

Since the "controller chip" and the "flash memories" are mounted on the substrate, it is a matter of technical common sense that they are connected to each other via a "wiring pattern." According to the configurations indicated above, the product disclosed in the known document is obviously a "semiconductor device."

Therefore, the following technology described in the known document can be acknowledged from the known document.

n The semiconductor device including:
a first to eighth flash memories;
b ninth to 16th flash memories;
c a controller for controlling the first to 16th flash memories;
d signal lines for connecting the controller to each of the first to 16th flash memories;
e and a substrate,
f the substrate including

j a rear surface side with a wiring pattern formed on a rear surface of the substrate and having the first to eighth flash memories and the controller mounted thereon,
k a front surface side with a wiring pattern formed on a front surface of the substrate and having the ninth to 16th flash memories mounted thereon,
l and a connector,
m and configured so that the first to eighth flash memories and the ninth to 16th flash memories are arranged substantially symmetrical with respect to the substrate.

Comparing the technology described in the known document with the Patent invention, the "signal line," which is the configuration d in the technology described in the known document, connects the "controller" to the "flash memories." However, the known document does not indicate that a "substrate" includes "resistive elements," or include descriptions about a signal line for connecting the "controller" to the "resistive elements" and a signal line for connecting the "resistive elements" to the "flash memories."

Furthermore, it cannot be observed from the known document that the "signal line" is "branched", that the "substrate" has an "internal wiring layer," or that the "branched" "signal line" "has a portion passing through the internal wiring layer."

Accordingly, the technology described in the known document does not have the following constituent components in the Patent invention.

- "The first to n-th resistive elements" (Constituent component C)
- The first to n-th signal lines for connecting the controller to each of the first to n-th resistive elements (Constituent component E)
- The (n+1)-th to 2n-th signal lines for connecting the first to n-th resistive elements to the first to n-th nonvolatile semiconductor memories, respectively (Constituent component F)
- The (2n+1)-th to 3n-th signal lines branched from the (n+1)-th to 2n-th signal lines and connected to the (n+1)-th to 2n-th nonvolatile semiconductor memories, respectively (Constituent component G)
- A front surface layer with a wiring pattern formed on a front surface of the substrate, and having the first to n-th nonvolatile semiconductor memories, the first to n-th resistive elements, and the controller mounted thereon (Constituent component J)
- including an internal wiring layer with a wiring pattern arranged between the front surface layer and the rear surface layer, and configured so that the (2n+1)-th to 3n-th signal lines have portions passing through the internal wiring layer (Constituent

component O).

It cannot be said that the constituent components were technical common sense for a person skilled in the art at the time of filing the application for the patent, in consideration of the contents alleged by the demandee in the cited written reply. It cannot be said that a person skilled in the art in contact with the known document recognizes the constituent components substantially described in the known document, accordingly.

As described above, since it cannot be said that the known document includes all of the constituent components of the Patent invention, the Patent invention cannot be recognized as a known art with the technology described in the known document.

The allegation of the demandee in the written reply, on the assumption that the Patent invention is a known art, cannot be accepted.

No. 6. Closing

The Article A falls within the technical scope of the Patent invention.

Therefore, the decision shall be made as described in the conclusion.

January 30, 2017

Chief administrative judge: TAKAGI, Susumu
Administrative judge: ISHII, Shigekazu
Administrative judge: TSUJIMOTO, Yasutaka