Trial decision

Invalidation No. 2016-800120

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The case of the patent invalidation trial of the invention of Japanese Patent No. 5869058, entitled "Semiconductor Device and System", between the parties above has resulted in the following trial decision:

Conclusion

The corrections regarding the Scope of Claims of Japanese Patent No. 5869058 about Claims [21-31] after correction are approved as the corrected Scope of Claims attached to the written correction request.

The demand for trial of the case was groundless.

The costs in connection with the trial shall be borne by the Demandant.

Reason

No. 1 History of the procedures

1 History of the application of the patent

Jun. 30, 2014 Application (reference date for publishing unexamined application: Mar. 16, 2011)
Mar. 27, 2015 Notice of reasons for refusal (drafting date)
Apr. 28, 2015 Interview record
May 21, 2015 Written opinion, Written amendment
Jun. 19, 2015 Interview record
Jun. 22, 2015 Notice of reasons for refusal (drafting date)
Aug. 27, 2015 Written opinion, Written amendment
Nov. 6, 2015 Decision to grant a patent (drafting date)
Jan. 15, 2016 Registration of establishment

2 History of the trial for invalidation of the case
Oct. 20, 2016 [Demandant] Written demand for trial
Jan. 6, 2017 [Demandee] Written reply, Written correction request
Feb. 8, 2017 [Demandee] Written amendment
Apr. 12, 2017 [Demandant] Written refutation of the trial case
Jun. 9, 2017 Notification of matters to be examined (drafting date)
Aug. 23, 2017 [Demandee] Oral proceedings statement brief
Aug. 25, 2017 [Demandant] Oral proceedings statement brief
Aug. 31, 2017 Written notice (drafting date)
Sep. 7, 2017 Oral proceeding, Examination of evidence
Sep. 14, 2017 [Demandee] Written statement
Oct. 2, 2017 [Demandant] Written statement
Oct. 10, 2017 [Demandee] Written statement

No. 2 Suitability of the correction according to the request for correction

1 The object of the request for correction and the contents of correction

The gist of the request for correction of Jan. 6, 2017 by the Demandee of the present trial for invalidation case (hereinafter, referred to as "Correction") is one "to request correction of the Scope of Claims of Japanese Patent No. 5869058 as the corrected Scope of Claims attached to the written demand of the case regarding Claims 21-31 after correction".

(1) Regarding a group of claims

Regarding Claims 21 to 31 before correction, since Claims 22 to 31 are ones that directly or indirectly refer to Claim 21, and are ones that are corrected in conjunction with Claim 21 whose recitation is corrected by the matters of correction, Claims 21 to 31 of Correction that correspond to Claims 21 to 31 before correction are a group of claims having a relation stipulated in Article 134-2(3) of the Patent Act.

(2) Regarding the matters of correction

"A plurality of wiring layers to be formed as an inner layer" recited in Claim 21 of the Scope of Claims is corrected to "a wiring layer to be formed as an inner layer comprising three plane layers as ground or power, and three signal layers for transmitting and receiving a signal".
(The underlined portions indicate corrected portions)

2 Judgment of suitability of correction

(1) Purpose of Correction

Since the matter of correction limits "a plurality of wiring layers to be formed as an inner layer" that is a matter specifying the invention of the invention according to Claim 21 before Correction to ones "comprising three plane layers as ground or power, and three signal layers for transmitting and receiving a signal", it is a correction for the purpose of "restriction of the Scope of Claims" stipulated in the Patent Act Article 134-2(1) proviso No. 1.

(2) Regarding new matters

Since it is described in paragraph [0015] of the description of the patent of the case that "The wiring layer 8b formed on each layer of the substrate 8 functions, as shown in FIG. 5, as a signal layer for transmitting and receiving a signal, and a plane layer to be a ground or power line.", the matter of correction has been made, when referring to FIG. 5 together, within the range of the matters described in the description of the patent of the case, and thus it complies with the provision of Article 126(5) of the Patent Act which is applied mutatis mutandis pursuant to Article 134-2(9) of the same Act.

(3) Regarding extension or change of the Scope of Claims

Since it is obvious that the matter of correction is not one that enlarges or alters the scope of claims, the matter of correction complies with the provision of Article 126(6) of the Patent Act which is applied mutatis mutandis pursuant to Article 134-2(9) of the same Act.

(4) Judgment on requirements for independent patentability

In the present case of the patent invalidation trial, since Claims 21 to 31 are the targets of the demand for trial for invalidation, the requirement of "must be one which should be independently patentable at the time of the patent application" stipulated in Article 126(7) of the Patent Act which is applied mutatis mutandis pursuant to Article 134-2(9) of the same Act is not applied to the correction concerning Claim 21 and the corrections concerning Claims 22 to 31 that directly or indirectly refer to Claim 21. Therefore, the correction concerning Claims 21 to 31 complies with the provision of Article 126(7) of the Patent Act which is applied mutatis mutandis pursuant to Article 134-2(9) of the same Act.

(5) Summary

As described above, Correction is for the purpose of the matter stipulated in Article 134-2(1) proviso No. 1 of the Patent Act, and complies with the provision of Article 126(5) to (7) of the same Act which is applied mutatis mutandis pursuant to Article 134-2(9) of the same Act; therefore, Correction is approved.

No. 3 The Patent Invention

Since Correction has been approved as the above-mentioned "No. 2", the inventions according to Claims 1 to 31 of the patent of the case (hereinafter, the

inventions according to each claim are respectively referred to as "Patent Invention 1", "Patent Invention 2", ... "Patent Invention 31"; in addition, these are collectively referred to as "the Patent Invention") are specified by the matters recited in Claims 1 to 20 of the Scope of Claims of the patent of the case, and Claims 21 to 31 of the Scope of Claims according to Correction as follows.

[Claim 1]

A semiconductor device comprising: a substrate; and a plurality of nonvolatile semiconductor memories mounted on the substrate, wherein

the substrate has

a first main surface, and a second main surface oriented opposite to the first main surface, and comprises

a first wiring layer provided on the first main surface, on which the plurality of nonvolatile semiconductor memories are mounted,

a second wiring layer provided on the second main surface,

a plurality of wiring layers to be formed as an inner layer, and

a plurality of insulation layers each provided between these wiring layers, wherein

one of the plurality of insulation layers is formed in an area including a center line of a layer structure of the substrate, wherein

a first value that is an absolute value of a difference between: a first average value that is an average value of wiring densities of the wiring layers formed in the side of the first main surface with respect to the center line of the layer structure of the substrate and the first wiring layer; and a second average value that is an average value of wiring densities of the wiring layers formed in the side of the second main surface with respect to the center line of the layer structure of the substrate and the second wiring layer is 7.5% or less, wherein

both the first average value and the second average value are 60% or more, wherein

a second value that is an absolute value of a difference between: a wiring density of the wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is formed in the side of the first main surface with respect to the center line of the layer structure of the substrate, and is proximate to the center line, and a wiring density of the wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is formed in the side of the second main surface with respect to the center line of the layer structure of the substrate and is proximate to the center line is larger than the first value, and wherein

at least one of the wiring layers among the plurality of wiring layers to be formed as an inner layer has a wiring density of 80% or more.

[Claim 2]

The semiconductor device according to Claim 1, wherein

a third wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the first wiring layer in a manner being separated by an insulation layer, has a wiring density of 80% or more.

[Claim 3]

The semiconductor device according to Claim 2, wherein

a fourth wiring layer, among the plurality of wiring layers to be formed as an

inner layer, that is opposite to the third wiring layer in a manner being separated by an insulation layer, and the first wiring layer are signal layers for sending and receiving a signal.

[Claim 4]

The semiconductor device according to Claim 2, wherein

a wiring density of the fourth wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the third wiring layer in a manner being separated by an insulation layer, is smaller than the first average value.

[Claim 5]

The semiconductor device according to Claim 1, wherein,

a fifth wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the second wiring layer in a manner being separated by an insulation layer, has a wiring density of 80% or more.

[Claim 6]

The semiconductor device according to Claim 1, wherein

at least one of the wiring layers among the plurality of wiring layers to be formed as an inner layer is a signal layer for sending and receiving a signal, and wherein

the signal layer is opposite to each of a sixth wiring layer and a seventh wiring layer having wiring densities of 80% or more among the wiring layers in a manner being separated by an insulation layer.

[Claim 7]

The semiconductor device according to Claim 2, wherein

an eighth wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the fifth wiring layer that is opposite to the second wiring layer in a manner being separated by an insulation layer, in a manner being separated by another insulation layer, has a wiring density smaller than the second average value.

[Claim 8]

The semiconductor device according to Claim 1, wherein

a surface of the first wiring layer is covered by solder resist.

[Claim 9]

The semiconductor device according to Claim 1, wherein

a surface of the second wiring layer is covered by solder resist.

[Claim 10]

The semiconductor device according to Claim 1, wherein

the nonvolatile semiconductor memory is a NAND type flash memory.

[Claim 11]

The semiconductor device according to Claim 10, wherein

four NAND type flash memories are mounted in the side of the first wiring layer of the substrate.

[Claim 12]

The semiconductor device according to Claim 1, wherein

the substrate has an approximately rectangular form in the top view.

[Claim 13]

The semiconductor device according to Claim 1, wherein

the first wiring layer, the second wiring layer, and the plurality of wiring layers to be formed as an inner layer include eight layers of wiring layers, and, among the eight layers of wiring layers, four layers are signal layers for sending and receiving a

signal, and the remaining four layers are wiring layers including ground or power lines.

[Claim 14]

A system comprising:

a substrate including a connector; a plurality of nonvolatile semiconductor memories mounted on the substrate; and a computer connected to the connector, wherein

the substrate has

a first main surface, and a second main surface oriented opposite to the first main surface, and comprises

a first wiring layer provided on the first main surface, on which the plurality of nonvolatile semiconductor memories are mounted,

a second wiring layer provided on the second main surface,

a plurality of wiring layers to be formed as an inner layer, and

a plurality of insulation layers each provided between these wiring layers, wherein

one of the plurality of insulation layers is formed in an area including a center line of a layer structure of the substrate, wherein

a first value that is an absolute value of a difference between: a first average value that is an average value of wiring densities of the wiring layers formed in the side of the first main surface with respect to the center line of the layer structure of the substrate and the first wiring layer; and a second average value that is an average value of wiring densities of the wiring layers formed in the side of the second main surface with respect to the center line of the layer structure of the substrate and the second wiring layer is 7.5% or less, wherein

both the first average value and the second average value are 60% or more, wherein

a second value that is an absolute value of a difference between: a wiring density of the wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is formed in the side of the first main surface with respect to the center line of the layer structure of the substrate, and is proximate to the center line, and a wiring density of the wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is formed in the side of the second main surface with respect to the center line of the layer structure of the substrate and is proximate to the center line is larger than the first value, and wherein

at least one of the wiring layers among the plurality of wiring layers to be formed as an inner layer is a shield layer.

[Claim 15]

The system according to Claim 14, wherein

the nonvolatile semiconductor memories are NAND type flash memories.

[Claim 16]

The system according to Claim 15, further comprising

a volatile memory electrically coupled to the nonvolatile semiconductor memories.

[Claim 17]

The system according to Claim 14, wherein

a third wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the first wiring layer in a manner being separated by an

insulation layer, has a wiring density of 80% or more.

[Claim 18]

The system according to Claim 17, wherein

a wiring density of the fourth wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the third wiring layer in a manner being separated by an insulation layer, is smaller than the first average value.

[Claim 19]

The system according to Claim 17, wherein

a sixth wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the fifth wiring layer that is opposite to the second wiring layer in a manner being separated by an insulation layer, in a manner being separated by another insulation layer, has a wiring density smaller than the second average value.

[Claim 20]

The system according to Claim 14, further comprising

a power circuit mounted on the substrate, wherein

the computer inputs power to the connector, wherein

the connector supplies the input power to the power circuit, and wherein

the power circuit is configured to generate internal voltage from the input power, and supply the internal voltage to the nonvolatile semiconductor memories.

[Claim 21]

A semiconductor device comprising:

a substrate including a connector connectable to a computer; a drive control circuit electrically coupled to the connector mounted on the substrate; and a plurality of nonvolatile semiconductor memories controlled by the drive control circuit, wherein

the substrate has

a first main surface, and a second main surface oriented opposite to the first main surface, and comprises

a first wiring layer provided on the first main surface,

a second wiring layer provided on the second main surface,

a wiring layer to be formed as an inner layer comprising three plane layers as ground or power, and three signal layers for transmitting and receiving a signal, and

a plurality of insulation layers each provided between these wiring layers, wherein

one of the plurality of insulation layers is formed in an area including a center line of a layer structure of the substrate, wherein

a first value that is an absolute value of a difference between: a first average value that is an average value of wiring densities of the wiring layers formed in the side of the first main surface with respect to the center line of the layer structure of the substrate and the first wiring layer; and a second average value that is an average value of wiring densities of the wiring layers formed in the side of the second main surface with respect to the center line of the layer structure of the substrate and the second wiring layer is 7.5% or less, wherein

both the first average value and the second average value are 60% or more, wherein

a second value that is an absolute value of a difference between: a wiring density of the wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is formed in the side of the first main surface with respect to the center line of

the layer structure of the substrate, and is proximate to the center line, and a wiring density of the wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is formed in the side of the second main surface with respect to the center line of the layer structure of the substrate and is proximate to the center line is larger than the first value, wherein

at least one of the wiring layers among the plurality of wiring layers to be formed as an inner layer has a wiring density of 80% or more, and wherein

the drive control circuit is mounted on the first main surface of the substrate.

[Claim 22]

The semiconductor device according to Claim 21, wherein

the plurality of nonvolatile semiconductor memories are provided in a side opposite to the connector seen from a position of the drive control circuit in a top view.

[Claim 23]

The semiconductor device according to Claim 21 or 22, wherein

the plurality of nonvolatile semiconductor memories are NAND type flash memories.

[Claim 24]

The semiconductor device according to any one of Claims 21 to 23, further comprising

a volatile memory electrically coupled to the drive control circuit.

[Claim 25]

The semiconductor device according to Claim 21, wherein

a third wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the first wiring layer in a manner being separated by an insulation layer, has a wiring density of 80% or more.

[Claim 26]

The semiconductor device according to Claim 25, wherein

a wiring density of the fourth wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the third wiring layer in a manner being separated by an insulation layer, is smaller than the first average value.

[Claim 27]

The semiconductor device according to Claim 25, wherein

a sixth wiring layer, among the plurality of wiring layers to be formed as an inner layer, that is opposite to the fifth wiring layer that is opposite to the second wiring layer in a manner being separated by an insulation layer, in a manner being separated by another insulation layer, has a wiring density smaller than the second average value.

[Claim 28]

The semiconductor device according to Claim 24, wherein

the connector is provided in a short side of the substrate, and

the volatile memory is provided in a side the same as that of the connector seen from the plurality of nonvolatile semiconductor memories in the top view.

[Claim 29]

The semiconductor device according to any one of Claims 21 to 28, further comprising

an LED for displaying a state of the semiconductor device.

[Claim 30]

The semiconductor device according to Claim 21, further comprising

a volatile memory mounted on the first main surface of the substrate, wherein

the substrate has an approximately rectangular form in a top view,

the plurality of nonvolatile semiconductor memories are four NAND type flash memories, and are mounted on the first main surface of the substrate in a side opposite to the volatile memory seen from a position of the drive control circuit in a top view, and wherein

the volatile memory, the drive control circuit, and the four NAND type flash memories are arranged in a long side direction of the substrate.

[Claim 31]

The semiconductor device according to Claim 30, wherein

the connector is provided in the short side of the substrate in a side opposite to the drive control circuit seen from the position of the volatile memory in the top view, and wherein

the connector, the volatile memory, the drive control circuit, and the four NAND type flash memories are arranged in a long side direction of the substrate.

No. 4 Allegations of the parties

1 The Demandant's allegation

(1) Object of the demand, Outline

The object of the demand is to demand a trial decision that the patent for the inventions according to Claim 1 to Claim 31 of the Scope of Claims of Japanese Patent No. 5869058 shall be invalidated, and the costs in connection with the trial shall be borne by the Demandee.

<Reason for invalidation 1>

The patent of the case is a divisional application from Japanese Patent Application No. 2011-058140 (hereinafter, referred to as "Original Application"). The patent of the case includes a concept and a description that are not described in the description originally attached at the time of the application of Original Application, and thus it is one to which a new matter is added with respect to the description originally attached at the time of the application of Original Application, which is inhibited by Article 17-2(3) of the Patent Act; therefore, the application date of Original Application is not adopted as the application date of the patent of the case. Accordingly, since the patent of the case is one for which the Demandee should not be granted a patent in accordance with the provisions of Article 29(1)(iii) of the Patent Act due to Original Application as the prior literature, the patent thereof falls under Article 123(1)(ii) of the Patent Act, and should be invalidated.

<Reason for invalidation 2>

The inventions according to Claims 1-31 of the patent of the case exceed the range described in the detailed description of the invention, and do not meet the requirement stipulated in Article 36(6)(i) of the Patent Act; therefore, the patents fall under Article 123(1)(iv) of the same Act, and should be invalidated.

<Reason for invalidation 3>

Since the inventions according to Claims 1-31 of the patent of the case do not

meet the requirement stipulated in Article 36(4)(i) of the Patent Act, the patents fall under Article 123(1)(iv) of the same Act, and should be invalidated.

<Reason for invalidation 4>

The inventions according to Claims 1-31 of the patent of the case are ones that are identical with the inventions described in Evidence A No. 1, and thus the Demandee should not be granted a patent for these in accordance with the provisions of Article 29(1)(ii) of the Patent Act, or these are ones that could have been invented by a person skilled in the art with ease in advance of the application based on the invention described in Evidence A No. 1 and thus the Demandee should not be granted a patent for these in accordance with the provisions of Article 29(2) of the Patent Act; therefore, the patents fall under Article 123(1)(ii) of the same Act, and should be invalidated.

In this regard, however, in the oral proceedings statement brief as of Aug. 25, 2017, the Demandant has alleged that "reason for invalidation 3 is withdrawn", and thus reasons for invalidation becomes reason for invalidation 1, reason for invalidation 2, and reason for invalidation 4.

(2) Evidence A submitted by the Demandant

Evidence A No. 1-1 A product analysis report

Evidence A No. 1-2 A product analysis report (Wiring density calculation method)

Evidence A No. 1-3 Transcend Information, Inc., 2010 Product catalog

Evidence A No. 1-4 TS256GSSD25S-M Product web page

Evidence A No. 1-5 TS512GSSD25S-M Product web page

Evidence A No. 1-6 An article entitled "Transcend Information, Inc., Read 260 MB/sec. Large capacity 512 GB SSD"

Evidence A No. 1-7 An article entitled "Speeded up! Capacity increased! 512 GB SSD by Transcend Information, Inc."

Evidence A No. 2 Japanese Unexamined Patent Application Publication No. 2010-135418

Evidence A No. 3 Japanese Unexamined Patent Application Publication No. 2005-123493

Evidence A No. 4 Japanese Unexamined Patent Application Publication No. H07-202359

Evidence A No. 5 Japanese Unexamined Patent Application Publication No. 2004-342934

Evidence A No. 6 Japanese Unexamined Patent Application Publication No. 2009-267162

Evidence A No. 7 Pioneer Corporation, Technical paper, 2006, VOL 16-No. 1, "Analysis of Warpage and Deformation Mechanism at the time of Substrate Mounting and Heating"

Evidence A No. 8 Pioneer Corporation, Technical paper, 2008, VOL 18-No. 2, "Introduction Evaluation of Warpage Analysis System for Substrate according to Simulation"

Evidence A No. 9 Japanese Unexamined Patent Application Publication No. H09-275251

Evidence A No. 9-2	A presentation material of Patent 3267148
Evidence A No. 10	A design material of PCB29-8370
Evidence A No. 11	A fact experiment notarized document No. 2017-103
Evidence A No. 12-1	A manufacturing instruction of SSD (S/N: 240214-0223)
Evidence A No. 12-2	A trace report of SSD (S/N: 240214-0223)
Evidence A No. 12-3	An invoice of SSD (S/N: 240214-0223)
Evidence A No. 12-4	A warranty period (standard) of SSD (S/N:240214-0223)
Evidence A No. 13-1	A manufacturing instruction of SSD (S/N:446165-0520)
Evidence A No. 13-2	A trace report of SSD (S/N: 446165-0520)
Evidence A No. 13-3	An invoice of SSD (S/N: 446165-0520)
Evidence A No. 13-4	A warranty period (standard) of SSD (S/N: 446165-0520)
Evidence A No. 14-1	A manufacturing instruction of SSD (S/N: 498000-0109)
Evidence A No. 14-2	A trace report of SSD (S/N: 498000-0109)
Evidence A No. 14-3	An invoice of SSD (S/N: 498000-0109)
Evidence A No. 14-4	A warranty period (standard) of SSD (S/N: 498000-0109)
Evidence A No. 15-1	A manufacturing instruction of SSD (S/N: 498739-0223)
Evidence A No. 15-2	A trace report of SSD (S/N: 498739-0223)
Evidence A No. 15-3	An invoice of SSD (S/N: 498739-0223)
Evidence A No. 15-4	A warranty period (standard) of SSD (S/N: 498739-0223)
Evidence A No. 16	An article of a product report
Evidence A No. 17-1	A manufacturing instruction of SSD (S/N: 347811-0005)
Evidence A No. 17-2	A trace report of SSD (S/N: 347811-0005)
Evidence A No. 17-3	An invoice of SSD (S/N: 347811-0005)
Evidence A No. 18-1	A manufacturing instruction of SSD (S/N: 397069-0006)
Evidence A No. 18-2	A trace report of SSD (S/N: 397069-0006)
Evidence A No. 18-3	An invoice of SSD (S/N: 397069-0006)
Evidence A No. 19	An article of a product report
Evidence A No. 20	The Print Circuit Technical Term Dictionary
Evidence A No. 21	The Reader of Printed Wiring Technology, second version
Evidence A No. 22	The Printed-wiring Board Technology
Evidence A No. 23	The Manufacturing Technology of Printed-wiring Board
Evidence A No. 24	Development of Ultrahigh Multilayer Substrate
Evidence A No. 25	A data sheet of DRAM (TMS4116)
Evidence A No. 26	Design Technique for EMC (second version), Sec. 5: Design and Layout of Printed Circuit Board
Evidence A No. 27	Mounting Technique of Multilayer Printed-wiring board
Evidence A No. 28	A product report article according to a product borrowed from the Demandant
Evidence A No. 29-1	A manufacturing instruction of SSD (S/N: 358462-0003)
Evidence A No. 29-2	A trace report of SSD (S/N: 358462-0003)
Evidence A No. 29-3	An invoice of SSD (S/N: 358462-0003)
Evidence A No. 29-3-2	A lending invoice of SSD (S/N: 358462-0003)
Evidence A No. 29-4	A warranty period (standard) of SSD (S/N: 358462-0003)

2. The Demandee's allegation

(1) Object of the reply

The object of the reply is to demand a trial decision that the demand for trial

of the case was groundless, and the costs in connection with the trial shall be borne by the Demandant.

(2) Evidence B submitted by the Demandee

Evidence B No. 1	Advisory Opinion 2016-600009
Evidence B No. 2	A product description of TS64GSSD25S-M
Evidence B No. 3	A product description of TS128GSSD25S-M
Evidence B No. 4	A product analysis report
Evidence B No. 5	Part Number Decoder
Evidence B No. 6	JMF616 Product Explanatory Document
Evidence B No. 7	Japanese Unexamined Patent Application Publication No. 2010-79445
Evidence B No. 8	A delivery slip
Evidence B No. 9	A receipt
Evidence B No. 10	Tracking
Evidence B No. 11	Russia - Send and take a look inside the world's postal situation
Evidence B No. 12	Demandant's warranty provisions
Evidence B No. 13	Product verification
Evidence B No. 14	Product verification
Evidence B No. 15	Product verification
Evidence B No. 16	A written reply to the advisory opinion request

No. 5 Judgment by the body

1 Regarding reason for invalidation 1 (addition of new matters)

The Demandant alleges as follows in the written demand for trial (page 22 to page 26). "In the description originally attached at the time of the application of Original Application, there is no description or concept to mean an upper limit or a lower limit with respect to a wiring density of copper foil in a wiring layer, such as 'or more', 'or less', 'greater than', or 'smaller than'. However, in Claim 1, Claim 14, and Claim 21 that are independent claims of the Scope of Claims of the patent of the case, there are recitations, regarding a wiring density, of '7.5% or less', '60% or more' ('80% or more'), and these are ones that indicate an upper limit or a lower limit of a wiring density. Therefore, the patent of the case is one that includes a description or concept that is not described in the description originally attached at the time of the application of Original Application, and thus it is one that adds a new matter, which is inhibited by Article 17-2(3) of the Patent Act, with respect to the description originally attached at the time of the application of Original Application; therefore, it is not one for which the application date of Original Application is adopted as the application date of the patent of the case."

Then, the allegation in question is examined.

In originally attached description of Original Application of the patent of the case, there are described the following matters. Note that, the underlines were applied by the body.

· [0005] An object of the present invention is to provide a semiconductor device that can suppress warpage of a substrate when a substrate of rectangular form in the top view is

used.

· [0014] FIG. 5 is a diagram showing a wiring density of each layer of the substrate 8. Here, the first layer to the fourth layer formed in the side of the surface layer with respect to the center line 30 (also refer to FIG. 4) of the layer structure of the substrate 8 are referred to as the upper layer, and the fifth layer to the eighth layer formed in the side of the rear surface layer with respect to the center line 30 are called the lower layer.

· [0015] The wiring layer 8b formed on each layer of the substrate 8 functions, as shown in FIG. 5, as a signal layer for transmitting and receiving a signal, and a plane layer to be a ground or power line. Then, a wiring density of wiring patterns formed on each layer; that is, a rate of an area occupied by the wiring layer to the surface area of the substrate 8, is configured as shown in FIG. 5.

· [0016] In the present embodiment, by making the eighth layer that functions as ground be a netlike wiring layer, instead of making it be a plane layer, the wiring density thereof is suppressed to 30 to 60%. Here, the wiring density of the substrate 8 as the whole upper layer is about 60%. Therefore, by forming a wiring pattern by making a wiring density of the eighth layer be about 30%, a wiring density of the lower layer as a whole can be made to be about 60%, and thus the wiring density of the upper layer as a whole and the wiring density of the lower layer as a whole can be made approximately equal. In this connection, by adjusting the wiring density of the eighth layer in a range of about 30-60%, the wiring density of the overall lower layer should just be made to be approximately equal to the wiring density of the overall upper layer.

· [0024] In the present embodiment, since the wiring density of the eighth layer is adjusted in a range of about 30-60%, and the wiring density of the overall upper layer is made approximately equal to the wiring density of the overall lower layer, thermal expansion coefficients of the two also become approximately equal to each other. For that reason, it is possible to prevent warpage of the substrate 8. In addition, since the wiring density is adjusted at the eighth layer that is furthest departed from the center line 30 (also refer to FIG. 4), occurrence of a moment for suppressing warpage can be made larger.

· [0028] Incidentally, in the present embodiment, although the wiring layer of the eighth layer is made to be a netlike wiring layer in order to adjust the wiring density of the overall lower layer of the substrate 8, the wiring layer may be formed, for example, on lines without being limited to the former. Furthermore, the wiring density of a layer in the lower layer other than the eighth layer; that is, a wiring layer from the fifth layer to the seventh layer, may be adjusted in order to adjust the wiring density of the lower layer as a whole. Of course, adjustment of a wiring density may be performed to all layers of the fifth layer to the eighth layer in order to adjust the wiring density of the lower layer as a whole.

Here, according to paragraphs [0005] and [0024], the object described in the originally attached description of Original Application is to "prevent warpage of a substrate", and, for that object, "the average values of the wiring density of the overall upper layer and the overall lower layer are made approximately equal". Specifically, as described in paragraphs [0014] to [0016], and [0024], the average of the wiring density of the overall lower layer becomes about 60% when the wiring density of the eighth layer is made to be the minimum value, 30%, and a difference between that and the average of wiring density of the overall upper layer becomes the minimum value, 0, and, when the wiring density of the eighth layer is made to be the maximum value, 60%,

the wiring density of the overall lower layer becomes about 67.5%, and "the maximum difference 7.5%" is generated between that and the average of wiring density of the overall upper layer. Therefore, the matter specifying the Invention of "a first value is 7.5% or less" of Patent Invention 1, Patent Invention 14, and Patent Invention 21 is a matter that is described in the description and drawings at the time of the application of Original Application.

In addition, as described above, it is described, in the originally attached description, etc. of Original Application, that prevention of warpage of a substrate can be accomplished by making the average value of the wiring densities of the upper layer as a whole and the average value of the wiring densities of the lower layer as a whole be approximately equal (the first value is 7.5% or less), and in light of the description, it cannot be read from the originally attached description, etc. of Original Application that making a wiring density of each layer, average values of the wiring densities of the overall upper layer and the overall lower layer be in predetermined ranges, respectively, is a direct purpose for preventing warpage of a substrate, and thus it is recognized that it is a matter that just limits the Scope of Claims within the range described in the description, etc. Then, in FIG. 5 at the time of the initial application of Original Application, it is described that the average of the wiring densities of the overall upper layer is about 60%, and the average of the wiring densities of the overall lower layer is about 67.5%, and thus it can be deemed that there is described a fact that each of the averages of wiring densities is 60% or more. Therefore, the matter specifying the invention of Patent Invention 1, Patent Invention 14, and Patent Invention 21 that "both the first average value and the second average value are 60% or more" is described in the description and drawings at the time of the initial application of Original Application. Further, as described in FIG. 5 at the time of the initial application of Original Application, wiring densities of plane layers (GND, Power) are about 80%, and, in paragraph [0030], it is disclosed that outermost layers or an inward layer may be a shield layer by covering the whole area thereof by copper foil (wiring density of 100%). Therefore, the matter specifying the invention of Patent Inventions 1 to 2, Patent Inventions 5 to 6, Patent Invention 17, Patent Invention 21, and Patent Invention 25 of "has a wiring density of 80% or more" is described in the description and drawings at the time of the initial application of Original Application.

Meanwhile, the Demandant also alleges that "substrates whose wiring densities are included in the recitation of the Scope of Claims by accident as a result of performing usual wiring design without devising so as not to cause warpage also come to be included in the technical scope. Since it cannot be deemed that such substrates are substrates liable to form warpage, these are not premised on the problem to be solved as suppressing warpage of a substrate, and thus the patent of the case substantially deviates from Original Application.". However, whether the patent of the case deviates from Original Application or not is a matter that is judged by whether or not it is within the range of the matter described in the description, the Scope of Claims, or the drawings at the time of the initial application of Original Application, and is not a matter that is judged by whether or not there is a substrate included in the Patent Invention by accident; therefore, the Demandant's allegation cannot be adopted. (If substrates whose wiring densities are included in the recitation of the Scope of Claims exist ordinarily, such evidence should be shown, and reasons for invalidation regarding novelty and inventive step should be alleged.)

Therefore, since the numerical values related to a wiring density of the Patent Invention are ones that are described in the description or drawings at the time of the initial application of Original Application, the patent of the case satisfies the requirements of division, and thus the reason for invalidation 1 of "the Demandee should not be granted a patent in accordance with the provisions of Article 29(1)(iii) of the Patent Act due to Original Application as the prior literature" cannot be adopted.

2 Regarding reason for invalidation 2 (violation of requirements for support)

The Demandant alleges as follows in the written demand for trial (page 26 to page 30).

In the Scope of Claims of the patent of the case, there are recitations regarding a wiring density as "7.5% or less", "60% or more", and "80% or more"; these are ones that indicate an upper limit or a lower limit of a wiring density. On the other hand, in paragraphs [0016] and [0024] of the detailed description of the invention, and FIG. 5 and FIG. 6, although there are descriptions of "about 60%-67.5%" and "about 30-60%", these are not ones that indicate a lower limit or an upper limit. Therefore, between the Scope of Claims of the Invention and the detailed description of the invention, there is no consistency in expression (formal correspondence relation).

Then, the allegation in question is examined.

Regarding the matters of paragraphs [0005], [0014] to [0016], [0024], [0028] and FIG. 5 of the originally attached description of Original Application, the same contents are described in paragraphs [0005], [0014] to [0016], [0024], and [0028] and FIG. 5 of the description of the case (strictly speaking, although paragraph [0005] is partially different, the underlined portions of paragraph [0005] that have been described in the above-mentioned "1" are common), and, therefore, as shown in the above-mentioned "1", the numerical values related to a wiring density of the Patent Invention ("7.5% or less", "60% or more", and "80% or more") are described in the description or drawings of the patent of the case.

Furthermore, the Demandant also alleges "non-existence of the problem to be solved as warpage", and "non-existence of a means for solving the problems in the Scope of Claims". However, the former allegation is the matter also alleged in the above-mentioned "1", and it is as having been judged in the above-mentioned "1". Also, regarding the latter allegation, as having judged in the above-mentioned "1", the constitution for solving the problem to be solved of the Patent Invention (to prevent warpage of a substrate) of "a first value is 7.5% or less" is described in the description, etc. of the patent of the case. Accordingly, the Demandant's allegation cannot be adopted.

Therefore, since the numerical values related to a wiring density of the Patent Invention are described in the description or drawings of the patent of the case, the reason for invalidation 2 that says that the Patent Invention "does not meet the requirement stipulated in Article 36(6)(i) of the Patent Act" cannot be adopted.

3 Regarding reason for invalidation 4 (a lack of novelty and inventive step)

The reasons for invalidation 4 is an allegation that the present invention is identical with the invention described in Evidence A No. 1 (Article 29(1)(ii) of the Patent Act), or could have been invented by a person skilled in the art with ease based on the invention described in Evidence A No. 1 (Article 29(2) of the Patent Act).

Then, Evidence A No. 1 will now be discussed below.

Although Evidences A No. 1-1 and 1-2 are described as a product analysis report, just photographs of images of the surface, the rear surface, each inner layer of a PCB substrate, and an image for calculating a wiring density are respectively posted, and there is no description about the relevant PCB substrate being embedded in what kind of product, and it is unclear. In addition, although Evidence A No. 1-3 to 1-7 are ones indicating that the product TSXXGSSD25S-M (in the position of XX, a numerical value showing the storage capacity, GB, of the product is filled) has been on the market generally before Mar. 16, 2011 that is the original filing date of the patent of the case, there is no indication at all in any of these about a PCB substrate used in the relevant product.

Although the Demandant alleges that "although TSXXGSSD25S-M as a demanded series started its release in year 2007, PCB29-7970 came into use in the product from Jul. 2010." (the written demand for trial, page 20), even carefully referring to the written demand for trial and Evidence A No. 1-1 to 1-7, there is no specific evidence that "PCB29-7970 analyzed in Evidence A No. 1-1 and 1-2" has been used in "TSXXGSSD25S-M that is supposed to have been sold from Jul., 2010", as pointed out by the body in the notification of matters to be examined as of Jun. 9, 2017.

In contrast to this, although the Demandant alleges, in the oral proceedings statement brief as of Aug. 25, 2017 and the written statement as of Oct. 2, 2017, showing new evidences (Evidence A No. 11 to Evidence A No. 29-4, in particular, the product of Evidence A No. 11 and the product of Evidence A No. 16), that "it is proved that TSXXGSSD25SM to which PCB29-7970 is mounted had been on the market in the general markets before Mar. 16, 2011 that is the priority date of the patent of the case", even if it is proved, there is no fact that "on all products of TSXXGSSD25S-M before priority date of the patent of the case, PCB29-7970 is used certainly"; therefore, only by indicating some pieces of TSXXGSSD25S-M on which PCB29-7970 is mounted, it cannot be proved that "PCB29-7970 analyzed in Evidence A No. 1-1 and Evidence A No. 1-2" is mounted on a product before the priority date of the patent of the case. Further, it remains unknown which product is a product on which PCB29-7970 analyzed in Evidence A No. 1-1 and Evidence A No. 1-2 is mounted.

In addition, even if the Demandant's allegation to the effect that it was manufactured in the 34th week (August) of Year 2010 because a numeral "1034" is printed on the bottom surface of the substrate of Evidence A No. 1-1 (the written demand for trial, pages 20-21) is admitted, there is no evidence that it was mounted on a product (SSD), and was on the market before Mar. 16, 2011. Regarding this point, although the Demandant alleges that a necessary period from manufacturing date of PCB29-7970 to shipping is one to three months (the oral proceedings statement brief as of Aug. 25, 2017, pages 7-8), it is a period that has been calculated from manufacturing to shipping of PCB substrates from the serial numbers of some products, it is not proved that this applies to all PCB substrates, and, further, the actual dates when they were put on the market have not been able to be proved; thus the Demandant's allegation cannot be adopted.

Therefore, since it is not recognized that the PCB substrates of Evidence A No. 1-1 and Evidence A No. 1-2 are publicly worked prior to the priority date of the patent of the case, the reason for invalidation 4 that says the Patent Invention does not have novelty and inventive step due to Evidence A No. 1 cannot be adopted.

In this connection, regarding Evidence A No. 11 that was submitted by the Demandant as evidence to "prove that TSXXGSSD25S-M on which PCB29-7970 is mounted had been on the market in the general market before Mar. 16, 2011 that is the priority date of the patent of the case", and for which examination of evidence was performed on Sep. 7, 2017, preliminary examination is now performed.

Evidence A No. 11 is made up of a fact experiment notarized document, photographs of a product and a PCB substrate, and Appendices 1 to 3. At the time of having performed the examination of evidence, a sealed package was opened, and it has been confirmed that the product is TS256GSSD25S-M (hereinafter, referred to as "A11 Product"), that the serial number is S/N: 411303-0009, and that the substrate contained in the interior portion when the package of A11 Product was opened is PCB29-7970. In this regard, however, on the substrate PCB29-7970, an element on which hand-written letters are described is mounted, and thus there is a doubt in a point that the package of A11 Product has been opened by a notary "for the first time", and, therefore, there is also a doubt whether the relevant substrate is the substrate mounted on the product at the time shipping.

Then, according to the manufacturing instruction (Work Order) of Appendix 1, the serial number trace report (S/T Trace Report) of Appendix 2, and the Invoice of Appendix 3 of Evidence A No. 11, and Evidence B No. 10, it is recognized that A11 Product is TS256GSSD25S-M on which PCB29-7970 is mounted, and arrived at Sheremetyevo International Airport, Russia, on Mar. 13, 2011.

However, as having been confirmed by the collegial body in the oral proceeding to the Demandant, the passing date of Russian customs clearance of A11 Product, and the date of arrival to 3R Memory are still unclear. In addition, in Russia, there is no proof that goods usually pass the customs clearance and arrive to a delivery destination in one or two days after having arrived at an airport.

Therefore, it is not recognized that A11 Product had been publicly worked prior to the priority date of the patent of the case.

Accordingly, Evidence A No. 11 is not evidence to "prove that TSXXGSSD25S-M on which PCB29-7970 is mounted had been on the market in the general market before Mar. 16, 2011 that is the priority date of the patent of the case".

No. 6 Closing

As above, the reasons alleged by the Demandant and the means of proof submitted by the Demandant cannot invalidate the patents according to Claims 1 to 31 of the patent of the case.

The costs in connection with the trial shall be borne by the Demandant under the provisions of Article 61 of Code of Civil Procedure which is applied mutatis mutandis pursuant to Article 169(2) of the Patent Act.

Therefore, the trial decision shall be made as described in the conclusion.

November 27, 2017

Chief administrative judge: MORIKAWA, Yukitoshi
Administrative judge: SAKAI, Tomohiro

Administrative judge: INOUE, Shinichi