Appeal decision

Appeal No. 2017-11744

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|---|---|
| Appellant | Hand Held Products, Inc. |
| Patent Attorney | ONO, Shinjiro |
| Patent Attorney | YAMAMOTO, Osamu |
| Patent Attorney | MIYAMAE, Toru |
| Patent Attorney | NAKANISHI, Motoharu |
| Patent Attorney | FUMA, Naoki |

The case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2015-227211, entitled "Image reading device with global electronic shutter control" (the application published on July 14, 2016, Japanese Unexamined Patent Application Publication No. 2016-129009) has resulted in the following appeal decision.

Conclusion

The appeal of the case was groundless.

Reasons

No. 1 History of the procedures

The present application is a divisional application filed on November 20, 2015 from Japanese Patent Application No. 2014-046409, which is a divisional application filed on March 10, 2014 from Japanese Patent Application 2013-003616, which is a divisional application filed on January 11, 2013 from Japanese Patent Application 2008-500844 filed on March 7, 2006 as an international filing date (priority claim under the Paris Convention: March 11, 2005 (hereinafter, referred to as "the priority date"), received by the foreign receiving office, United States), and the history of the subsequent procedures is as follows.

Dated October 19, 2016 Notification of reasons for refusal

March 24, 2017 Submission of written opinion and written amendment
Dated April 5, 2017 Examiner's decision of refusal
August 7, 2017 Submission of written request for appeal and written amendment
Dated January 12, 2018 Notification of reasons for refusal
July 13, 2018 Submission of written opinion and written amendment
Dated September 14, 2018 Notification of reasons for refusal
January 18, 2019 Submission of written opinion and written amendment

No. 2 Regarding the invention

The invention according to claims of the present application is as specified by the matters described in Claims 1 to 42 of the scope of claims which have been amended by the procedures of amendment as of January 18, 2019, and the invention according to Claim 1 (hereinafter, referred to as "the Invention") is as follows, as specified by the matters described in Claim 1.

"A device used for reading a bar code, the device comprising:

a two-dimensional image sensor array, the two-dimensional image sensor array being made from a complementary metal oxide semiconductor, the two-dimensional image sensor array containing rows of pixels;

an image pickup lens that focuses light on the two-dimensional image sensor array;

a support assembly, the support assembly containing a lens holder for supporting the image pickup lens;

an illumination light source used for projecting an illumination pattern, the illumination light source being made from a light-emitting diode; and

a global electronic shutter control module that is disposed so as to simultaneously expose a plural rows of pixels of the two-dimensional image sensor array during an exposure period, the global electronic shutter control module being configured to control the two-dimensional image sensor array so that the exposure of the plural rows of pixels in the two-dimensional image sensor array is simultaneously started,

wherein the device is characterized by the exposure period and an illumination period in which the light-emitting diode can be simultaneously driven during the illumination period, and adjustment between the exposure period and the illumination period is at least partially overlapped in time".

No. 3 Reasons for refusal

Reasons for refusal notified by the body on September 14, 2018 are as follows.

Since the Invention would have been easily made by a person who had ordinary skill in the art belonging to the Invention before the priority date, based on the inventions described in the following publications which had been distributed in Japan or a foreign country or inventions that had become available to the public through electric communication lines before the priority date, the Appellant should not be granted a patent for the Invention under the provisions of Article 29(2) of the Patent Act.

Cited Document 1. Japanese Unexamined Patent Application Publication No. 2003-132301

Cited Document 2. United States Patent Application Publication No. 2005/0001035

Cited Document 3. Japanese Unexamined Patent Application Publication No. H10-198754

Cited Document 4. Japanese Unexamined Patent Application Publication No. H11-345278

Cited Document 5. Japanese Unexamined Patent Application Publication No. 2003-87148

Cited Document 6. Japanese Unexamined Patent Application Publication No. 2002-240913

Cited Document 7. Japanese Unexamined Patent Application Publication No. 2005-22802

Cited Document 8. Japanese Unexamined Patent Application Publication No. 2001-357345

Cited Document 9. Japanese Unexamined Patent Application Publication No. 2003-260822

Cited Document 10. Japanese Unexamined Patent Application Publication No. H08-181887

Cited Document 11. Japanese Unexamined Patent Application Publication No. S59-40630

No. 4 Description in the Cited Documents and Cited Invention

1 Description of Cited Document 1

(1) Cited Document 1 describes the following matters (Underlines are added by the body, hereinafter the same.).

"[0001]
[Field of the Invention] The present invention relates to a bar code reading technique, and more particularly to a bar code reading technique using an image sensor"

"[0015]
[Embodiments of the invention] FIG. 1 is a block configuration diagram of a bar code reading device according to an embodiment of the present invention.
[0016] In FIG. 1, reference numeral 1 denotes a lens unit for forming a general subject image or a subject image of a bar code described in a black-and-white pattern on a sensor surface. Reference numerals 2 to 5 denote red light emitting diodes (LEDs) for illuminating bar codes, and in order to evenly illuminate the object to be photographed around the image sensor 1 with a sufficient amount of light, a total of 16 high-brightness red LEDs are arranged, 4 each for top, bottom, right, and left. Reference numeral 6 denotes an image pickup element portion and uses a CMOS type image sensor for generating a two-dimensional image by photoelectric conversion. Reference numeral 7 denotes a timing signal generator (TG) that supplies a drive clock to the image sensor 6, receives information on the exposure time calculated by a system control unit 8, and changes the exposure time of the image sensor 6 accordingly. Reference numeral 10 denotes an automatic gain control (AGC) amplifier that amplifies the image output signal of the image sensor 6, receives information on the amplification degree calculated by the system control unit 8, and changes the amplification degree accordingly. The image signal amplified by the amplifier 10 is quantized by an A/D converter denoted by reference numeral 11 and enters a signal processing unit (circuit) denoted by reference numeral 12. Here, the bar code signal is binarized, decoded, etc., the average value of the image signal is calculated, and the threshold value is sent to the system control unit 8. The system control unit 8 controls the on/off of the LED through an LED drive unit 9, and also decides the photoelectric conversion time information sent to the timing signal generation unit and the amplification degree information sent to the amplifier by the threshold value from the signal processing unit 12. The initial setting of the exposure time and the initial setting of the system control unit 8 are stored in ROM 18. Next, reference numeral 13 denotes an image memory for signal processing. In addition, when the decoding is completed, the information is transmitted to an external personal computer (personal computer) 14, displayed on a monitor 15, and transmitted to a buzzer 16 for transmitting the completion of decoding or a decoding error. It is also possible to prepare a recording medium 17 and store the

information that has been deciphered so far.

[0017] FIG. 3 is a block diagram of the CMOS type image sensor according to the present embodiment, and the sensor is composed of pixels S11 to Smn of m rows × n columns, but is not limited to m rows × n columns.

[0018] FIG. 4 is a detailed view of the pixels. In this figure, an anode side of a photodiode PD that generates the optical signal charges is grounded. A cathode side of the photodiode PD is connected to a gate of an amplification MOS transistor M3 via a charge transfer switch TX. Further, a source of the reset MOS transistor M1 for resetting the gate of the amplification MOS transistor M3 is connected to the gate of the amplification MOS transistor M3, and a drain of a reset MOS transistor M1 is connected to a reset voltage VR. Further, a drain of the amplification MOS transistor M3 is connected to a row selection MOS transistor M2 for supplying operating voltage VDD.

[0019] Next, the driving method of the solid-state image pickup device of the present embodiment will be described with reference to FIGS. 3, 4, and a timing diagram of FIG. 5.

[0020] A signal TXa that simultaneously selects the gates of transfer MOS transistors TX in FIG. 3 for all the pixels from the first row to the mth row is connected to each transfer MOS transistor TX through an OR circuit with transfer pulses TX1 to TXn of the signal that selects all the pixels for each row. Further, in order to simultaneously reset the gates of the amplification MOS transistors M3 of all the pixels, a signal RESa that simultaneously selects the gates of the reset MOS transistors M1 of all the pixels from the first row to the mth row is connected to each reset MOS transistor M1 through an OR circuit with pulses RES1 to RESn that reset the pixels for each row.

[0021] In this image sensor, first, a pulse φRESa to the gate of the reset MOS transistor M1, a gate pulse φTXa of the transfer MOS transistor TX, and the pulse φVRES to the gate of a vertical signal line reset MOS transistor M8 are at high levels. Therefore, the gate of the amplification MOS transistor M3 and the photodiode PD are reset to the voltage VR, and the vertical signal lines V1 to Vn are reset to the voltage VVR (up to t2 in FIG. 5).

[0022] Next, φTXa becomes low level, and the photodiode PD can generate an electric charge according to the light (t2). In the LED lighting mode, the control signal φLED becomes high level and the LED is lit prior to t2 (t1). Subsequently, the pulse φRESa to the gate of the reset MOS transistor M1 and the gate pulse φVRES of the vertical signal line reset MOS transistor M8 become low level, and the reset of the gate of M1 and the vertical signal line is released (t3). After a predetermined time from time t3,

φTXa is set to a high level again and the charge of the photodiode PD is transferred to the gate of the amplification MOS transistor M3 (t4).

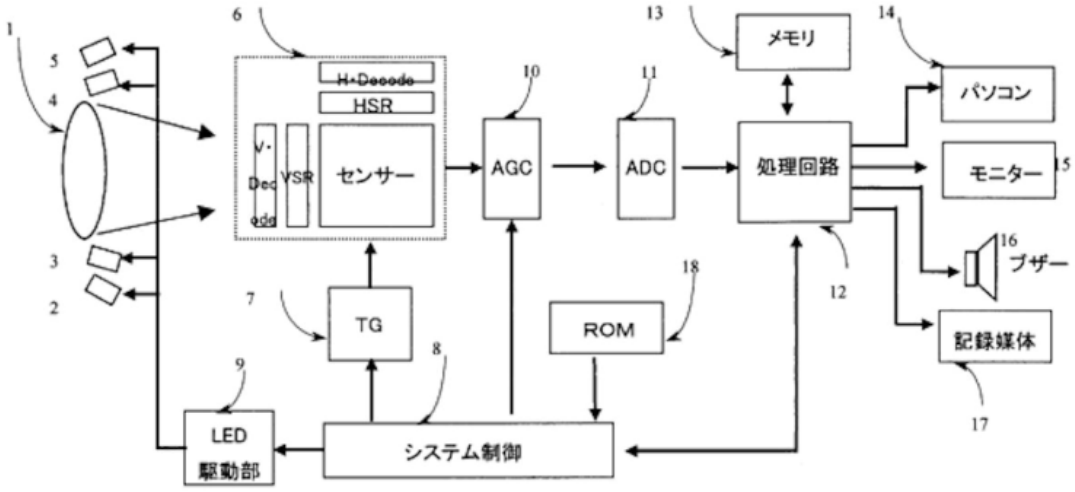
[0023] After a sufficient time for transfer, the φTXa is lowered again to end the charge transfer of the photodiode PD (t5). In this case, the photoelectric conversion time is between t2 and t5. In the mode in which the LED is turned on, the LED is turned off after the transfer is ended (t6). Next, the gate pulse φSEL1 of the selection MOS transistor M2 and the gate pulse φTS of the optical signal transfer MOS transistor M5 become high levels (t7). Therefore, the optical signal voltage is read out to the optical signal holding capacitance CTS (t7 to t8). After reading to the capacitive CTS, the pulse φRES1 to the gate of the reset MOS transistor M1 and the gate pulse φVRES of the reset MOS transistor M8 become high level, and the gate of M1 and the vertical signal line are reset (t9). Subsequently, φRES1 and φVRES become low level (t10), and after the reset of the gate of M1 and the vertical signal line is released, the gate pulse φSEL1 of the selection MOS transistor M2 and the gate pulse φTN of a noise signal transfer MOS transistor M4 become high level (t11). Therefore, the noise voltage is read out to the optical signal holding capacitance CTN (t11 to t12). After that, the gates of the horizontal transfer switches M6 and M7 in each row are sequentially raised to a high level by the signals H1 to Hn from the horizontal scanning circuit block HSR, and voltage held in the noise holding capacitance CTN and the optical signal holding capacitance CTS is sequentially read out to a differential circuit block (t14 to t15). In the differential circuit block, differences between the optical signal and the noise signal are taken, and are sequentially output to an output terminal VOUT.

[0024] With the above, the reading of the pixel cell connected to the first row is completed. After that, prior to the reading of the second line, φCTR to the gates of the reset switches M9 and M10 of the noise signal holding capacitance CTN and the optical signal holding capacitance CTS becomes high level and are reset to VRCT.

[0025] Similarly, the signals of the pixel cells C21 to Cmn connected to the second row to the mth row are sequentially read out by the signals from the vertical scanning circuit block VSR, and the reading of all the pixel cells is completed.

[0026] From the above operation explanation, such a CMOS image sensor does not require scanning for one screen when returning from the sleep state of the sensor, and the start-up is completed only by a batch reset, low power consumption drive is possible without requiring a high-speed pulse, and the sensor can be started up early until the bar code is read".

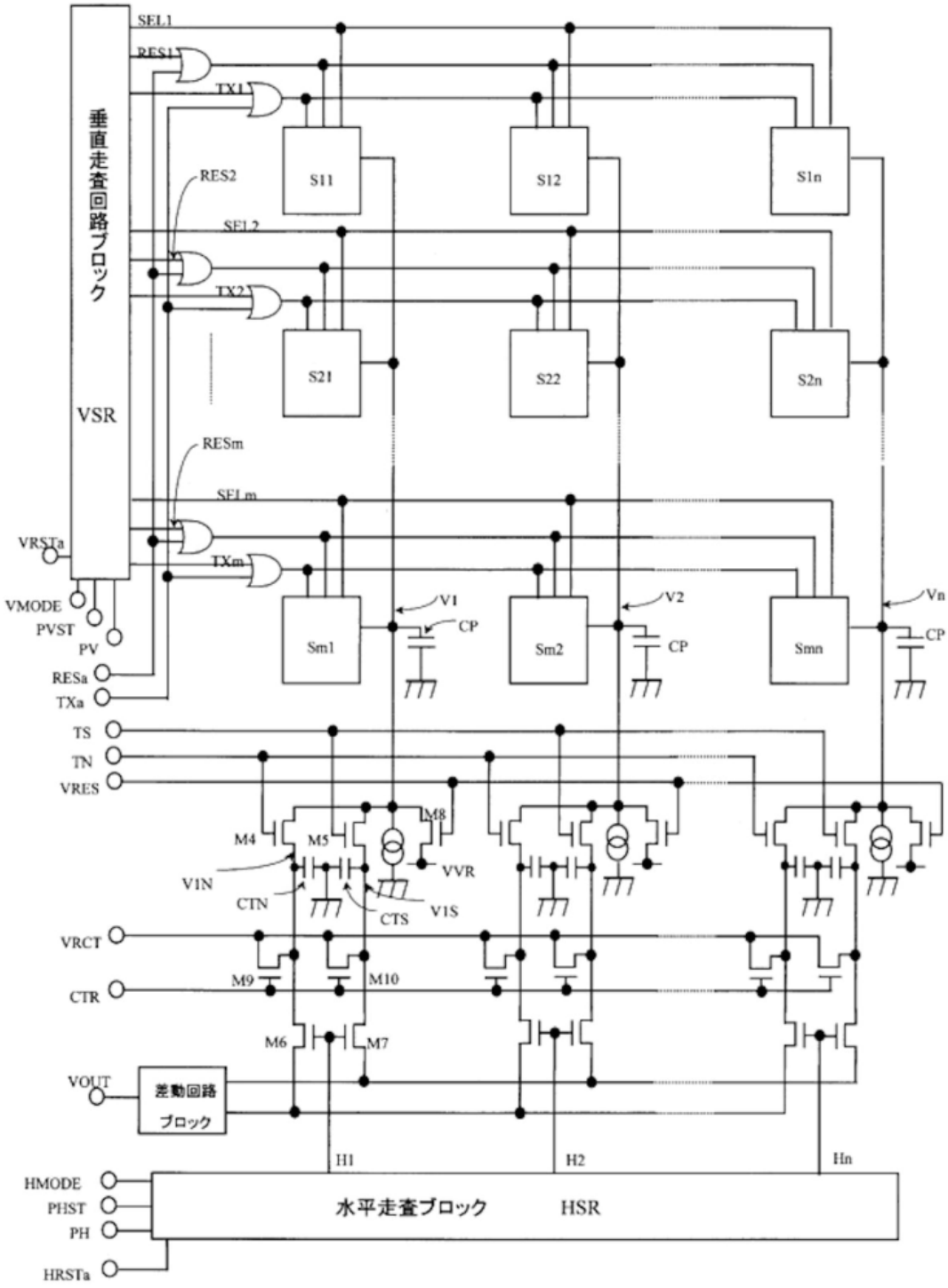
[FIG.1]




本実施形態のシステム構成図

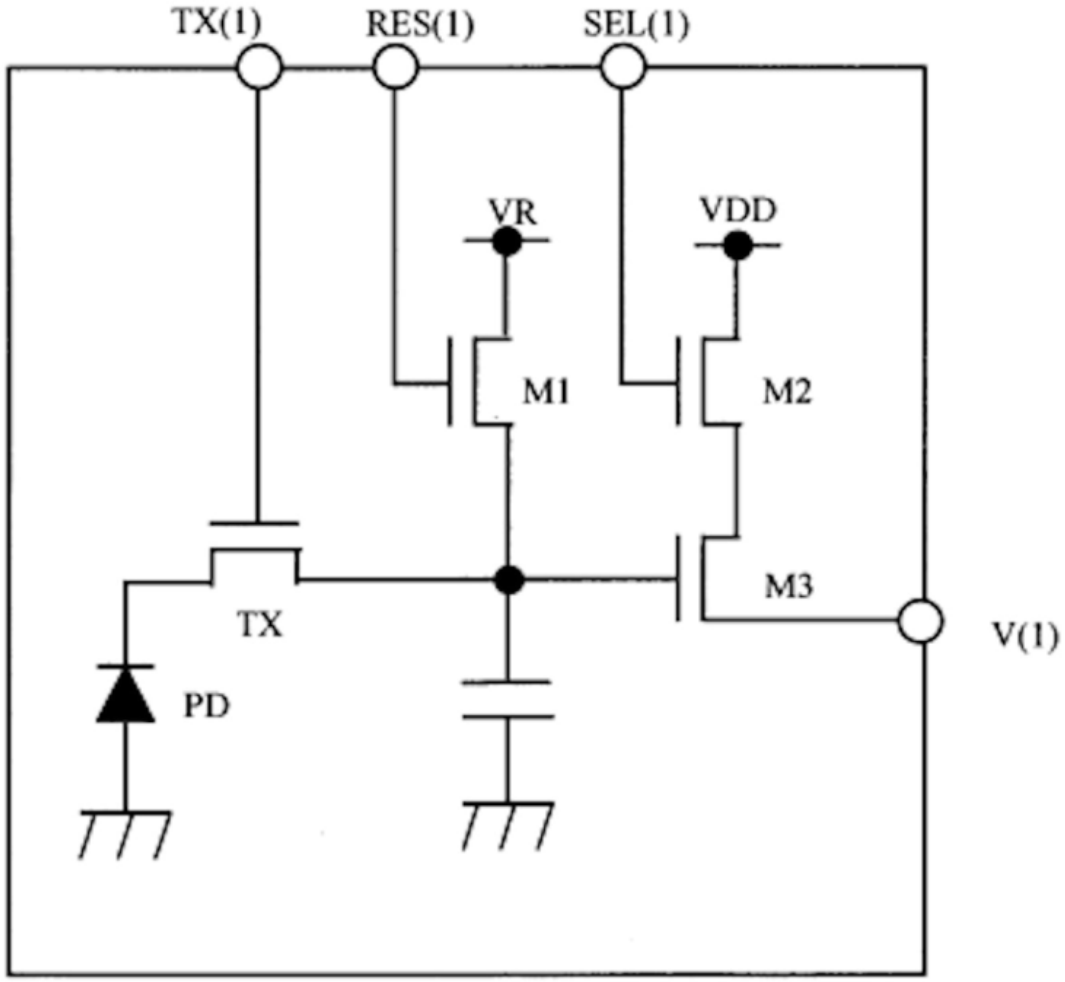
| | |
|---|---|
| センサー | Sensor |
| メモリ | Memory |
| 処理回路 | Processing circuit |
| パソコン | Personal computer |
| モニター | Monitor |
| ブザー | Buzzer |
| 記録媒体 | Recording medium |
| LED駆動部 | LED Driving unit |
| システム制御 | System control |
| 本実施形態のシステム構成図 | System configuration diagram |

[FIG. 3]




垂直走査回路ブロック　Vertical scanning circuit block
差動回路ブロック　Differential circuit block
水平走査ブロック　Horizontal scanning block

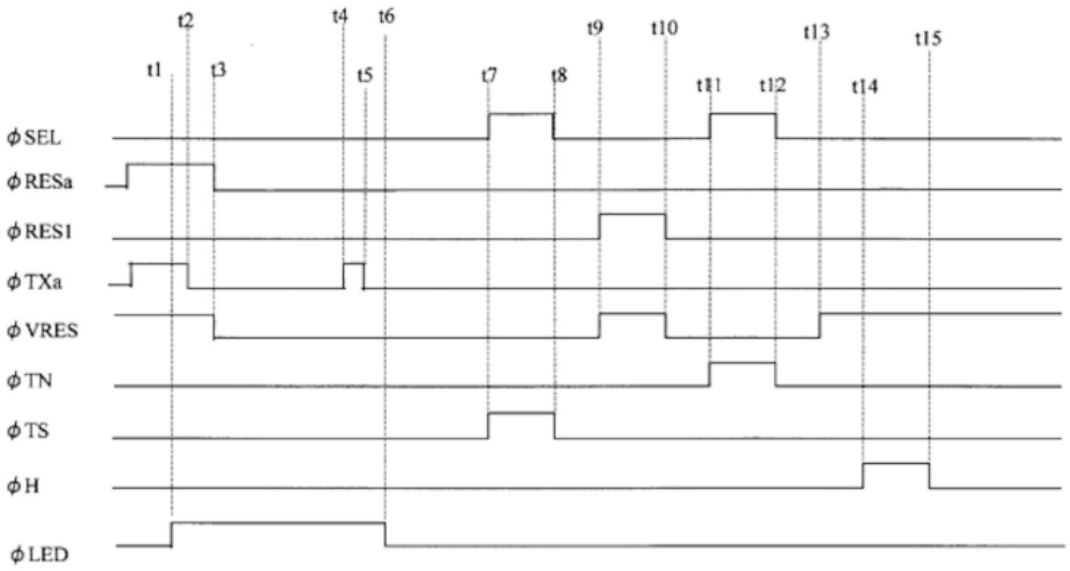
[FIG. 4]




画素部構成部

画素部構成部　　Pixel portion configuration unit

[FIG. 5]




センサー駆動タイミング図

**センサー駆動タイミング図**　　Sensor drive timing diagram

(2) From (1) above, Cited Document 1 describes the following matters.

A　According to the description of "φTXa becomes low level, and the photodiode PD can generate an electric charge according to the light (t2)" (Paragraph [0022]) of Cited Document 1, and the description of the configuration in which "TXa" corresponding to the signal "φTXa" in [FIG. 3] is input to all "pixels S11 to Smn" through the OR circuit, in Cited Document 1, as of t2 of [FIG. 5], "a charge transfer switch TX" of "a pixel portion configuration unit" shown in [FIG. 4] is turned off in all "pixels S11 to Smn" and "the optical signal charges" are accumulated on a cathode side of "the photodiode PD".

B　Then, according to the description "the pulse φRESa to the gate of the reset MOS transistor M1 and the gate pulse φVRES of the vertical signal line reset MOS transistor M8 become low level, and the reset of the gate of M1 and the vertical signal line is released (t3)" (Paragraph [0022]) of Cited Document 1, and the description of the configuration in which "RESa" corresponding to the signal "φRESa" in [FIG. 3] is input to all "pixels S11 to Smn" through the OR circuit, in Cited Document 1, as of t3 of [FIG. 5], "the reset of the gate of M1" of "the pixel portion configuration unit" shown in [FIG. 4] is turned off in all "pixels S11 to Smn" and the reset is released.

C　After that, according to the description "after a predetermined time from time t3,

φTXa is set to a high level again and the charge of the photodiode PD is transferred to the gate of the amplification MOS transistor M3 (t4)," the description of "a photodiode PD that generates the optical signal charge" (Paragraph [0018]), and the configuration described in "A" above of [FIG. 3], in Cited Document 1, as of t4 of [FIG. 5], "a charge transfer switch TX" of "a pixel portion configuration unit" shown in [FIG. 4] is turned on in all "pixels S11 to Smn" and "the optical signal charge" accumulated on a cathode side of "the photodiode PD" is transferred to the gate of "the amplification MOS transistor M3".

D According to the description "after a sufficient time for transfer, the φTXa is lowered again to end the charge transfer of the photodiode PD (t5)" (Paragraph [0023]) and the configuration described in "A" above of [FIG. 3], in Cited Document 1, as of t5 of [FIG. 5], "a charge transfer switch TX" of "a pixel portion configuration unit" shown in [FIG. 4] is turned off in all "pixels S11 to Smn" and the transfer to the gate of "the amplification MOS transistor M3" of "the optical signal charge" accumulated on a cathode side of "the photodiode PD" is ended.

E As shown in A-D above, it can be said that Cited Document 1 describes the configuration in which during "the photoelectric conversion time" between t2 and t5 of [FIG. 5] (Paragraph [0023]), "the optical signal charges" are accumulated on a cathode side of "the photodiode PD" simultaneously as of t2 in all "pixels S11 to Smn," then the accumulated "optical signal charges" are simultaneously transferred to the gate of "the amplification MOS transistor M3" since t3, and then the transfer to the gate of "the amplification MOS transistor M3" of "the optical signal charges" is simultaneously ended as of t5.

F According to the description "the gate pulse φSEL1 of the selection MOS transistor M2 and the gate pulse φTS of the optical signal transfer MOS transistor M5 become high levels (t7). Therefore, the optical signal voltage is read out to the optical signal holding capacitance CTS (t7 to t8)" (Paragraph [0023]), and the description of the configuration in which "SEL1" corresponding to the signal "φSEL1" in [FIG. 3] is input to "S11 to S1n" that are pixels in the first row, it can be said that Cited Document 1 describes that "the selection MOS transistor M2" of "a pixel portion configuration unit" shown in [FIG. 4] is turned on in the pixels "S11 o S1n" in the first row, as of t7 of [FIG. 5], and the signal according to "the optical signal charge" transferred to the gate of "the amplification MOS transistor M3" of each pixel (S11 to S1n) in the first row is output from a drain side of "the amplification MOS transistor M3" as "optical signal voltage," is accumulated in "the optical signal holding capacitance CTS," and is read out.

G According to the descriptions of [FIG. 1] and Paragraph [0016], it is recognized that

"a timing signal generator" is equipped with "a timing signal generator (TG)".
H Further, it is recognized that "the optical signal holding capacitance CTN" and "the noise holding capacity CTN" in Paragraph [0023] is a misprint of "the noise signal holding capacitance CTN" in Paragraph [0024], and "the pixel cells C21 to Cmn" in Paragraph [0025] is a misprint of "the pixels cells S21 to Smn".

(3) According to (1) and (2) above, Cited Document 1 describes the following invention (hereinafter, referred to as "the Cited Invention").

"A bar code reading device, comprising:

a CMOS type image sensor for generating a two-dimensional image by photoelectric conversion, the image sensor 6 of an image pickup element portion being composed of pixels S11 to Smn of m rows × n columns;

a lens portion 1 for focusing a subject image on a sensor surface;

red light emitting diodes (LED) 2 to 5 for evenly illuminating an object to be photographed with a sufficient amount of light;

a system control unit 8 that decides photoelectric conversion time information sent to a timing signal generation unit; and

a timing signal generator (TG) 7 of the timing signal generation unit that supplies a drive clock to the image sensor 6,

wherein a gate of an amplification MOS transistor M3 of each pixel and a photodiode PD are reset to a voltage VR, and vertical signal lines V1 to Vn are reset to a voltage VVR,

wherein an LED is lit (t1),

wherein optical signal charges are simultaneously accumulated on a cathode side of the photodiode PD in all pixels S11 to Smn, then, the accumulated optical signal charges are simultaneously transferred to the gate of the amplification MOS transistor M3, and then the transfer to the amplification MOS transistor M3 of the optical signal charges is simultaneously ended (t2 to t5),

wherein the LED is turned off after the transfer is ended (t6),

wherein the optical signal voltage of pixels S11 to S1n in a first row is read out to an optical signal holding capacitance CTS (t7 to t8),

wherein a noise voltage is read out to a noise signal holding capacitance CTN (t11 to t12),

wherein voltage held in the noise signal holding capacitance CTN and the optical signal holding capacitance CTS are sequentially read out to a differential circuit

block, and differences between the optical signal and the noise signal are taken, and are sequentially output to an output terminal VOUT (t14 to t15), and

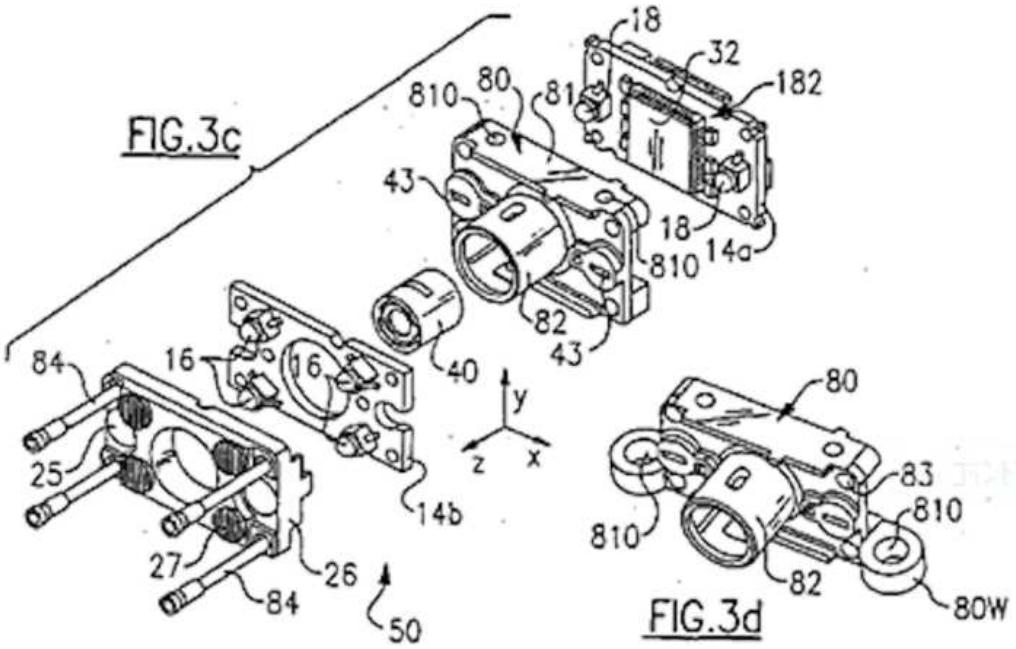
wherein, similarly, signals of the pixels S21 to Smn connected to a second row to an mth row are sequentially read out by signals from a vertical scanning circuit block VSR, and the reading of all the pixels is completed".

2 Cited Document 2

(1) Cited Document 2 describes the following matters

"[0002] This invention relates generally to optical readers and specifically to an optical reader configured to take pictures."

"[0030] An imaging module 50 which may be incorporated into a reader housing to form an optical reader is described with reference to FIGS. 3a-3d. The imaging module 50 may be an IT 4000 imaging module of the type available from Hand Held Products, Inc. of Skaneateles Falls, N.Y. IT4000 imaging modules available from Hand Held Products, Inc. are available with associated decode circuits which may be actuated to decode a decodable indicia, such as bar code indicia, within a captured image. The Imaging module 50 can be a IT4200 imaging module with an associated decode-out circuit, also available from Hand Held Products, Inc. The Imaging module 50 includes a support 80 having a containment 81 containing an image sensor 32 incorporated on a chip 182, and a retainer section 82 retaining a lens assembly 40 provided by a lens barrel. The lens assembly 40 includes a lens or lenses which focus images from a substrate (as seen in FIG. 3b) onto the image sensor 32. In one embodiment, the lens assembly 40 is configured so that the module 50 has a fixed best focus receive distance of less than two feet (e.g., 3 inches, 5 inches, 7 inches, 15 inches). Configuring the lens assembly 40 so that the module 50 has a best focus receive distance of less than two feet allows the module 50 to capture high resolution images at short range, from which decodable indicia can readily be decoded. The module 50 can also be configured so that the module 50 has a best focus distance of several feet such as 5 feet or more as is described in U.S. application Ser. No. 10/252,484, filed on Sep. 23, 2002, entitled "Long Range Optical Reader," incorporated by reference. The module 50 can also include an adjustable lens assembly for providing an adjustable best focus receive distance."




(2) According to (1) above, Cited Document 2 describes the following matter (hereinafter, referred to as "the matter described in Cited Document 2"), as an optical reading device for reading bar code indicia.

"An optical reader for reading a bar code, wherein an imaging module 50 capable of decoding bar code indicia includes a support 80 having a containment 81 containing an image sensor 32 incorporated on a chip 182, and a retainer section 82 retaining a lens assembly 40 provided with one or more lenses provided by a lens barrel".

No. 5 Comparison

Comparing the Invention with the Cited Invention, the following matters can be acknowledged.

1 "A bar code reading device" and "red light emitting diodes (LEDs) 2 to 5 for evenly illuminating an object to be photographed with a sufficient amount of light" of the Cited Invention correspond to "a device used for reading a bar code" and "an illumination light source used for projecting an illumination pattern, the illumination light source being made from a light-emitting diode" of the Invention, respectively.

2 "An image sensor 6" of the Cited Invention is "a CMOS type image sensor for generating a two-dimensional image by photoelectric conversion, the image sensor 6 being composed of pixels S11 to Smn of m rows × n columns," so that the matter that "a

image sensor 6" of the Cited Invention is "a CMOS type image sensor" corresponds to the matter that "the two-dimensional image sensor array is made from a complementary metal oxide semiconductor" of the Invention. Further, the matter that "the image sensor 6" of the Cited Invention is "composed of pixels S11 to Smn of m rows × n columns" corresponds to the matter that "the two-dimensional image sensor array contains rows of pixels" of the Invention.

Therefore, "an image sensor 6" of the Cited invention corresponds to "a two-dimensional image sensor array" of the Invention. Further, "a lens portion for focusing a subject image on a sensor surface" of the Cited Invention corresponds to "an image pickup lens that focuses light on the two-dimensional image sensor array" of the Invention.

3 Since it is described that "the photoelectric conversion time is between t2 and t5" in Paragraph [0023] of Cited Document 1, periods t2 to t5 of the Cited Invention correspond to "an exposure period" of the Invention. Then, in the Cited Invention, since "optical signal charges are simultaneously accumulated on a cathode side of the photodiode PD in all pixels S11 to Smn, then, the accumulated optical signal charges are simultaneously transferred to the gate of the amplification MOS transistor M3, and then the transfer to the amplification MOS transistor M3 of the optical signal charges is simultaneously ended," all pixels S11 to Smn are simultaneously exposed during "an exposure period" and thus it can be said that the Cited Invention also "simultaneously exposes a plurality of rows of pixels of the two-dimensional image sensor array, during an exposure period".

Further, since "all pixels S11 to Smn" of the Cited Invention are simultaneously started to be exposed as of t2, it can be said that also in the Cited Invention, "the exposure of the plural rows of pixels in the two-dimensional image sensor array is simultaneously started".

4 Since the matter that "optical signal charges are simultaneously accumulated on a cathode side of the photodiode PD in all pixels S11 to Smn, then, the accumulated optical signal charges are simultaneously transferred to the gate of the amplification MOS transistor M3, and then the transfer to the amplification MOS transistor M3 of the optical signal charges is simultaneously ended" of the Cited Invention means that the exposure is simultaneously started and the exposure is simultaneously ended in all pixels, it is recognized that the Cited Invention also realizes a global shutter.

Therefore, it can be said that "a system control unit 8 that decides

photoelectric conversion time information sent to a timing signal generation unit; and a timing signal generator (TG) 7 of the timing signal generation unit that supplies a drive clock to the image sensor 6" of the Cited Invention configures a control unit realizing the global shutter by controlling the accumulation and transfer of the optical signal charges of the Cited Invention, so that "a timing signal generator (TG) 7" and "a system control unit 8" of the Cited Invention correspond to "a global electronic shutter control module" of the Invention.

5 Since "red light emitting diodes (LED) 2 to 5" of the Cited Invention are lit as of t1 prior to t2 when starting the accumulation of the optical signal charges, are turned off as of t6 after t5 when the accumulation of the optical signal charges is ended, and are partially overlapped with "the exposure period" (t2 to t5) of the Cited Invention, it is recognized that the Cited Invention also has the period similar to "the exposure period and an illumination period in which the light-emitting diode can be simultaneously driven during the illumination period, and adjustment between the exposure period and the illumination period is at least partially overlapped in time" of the Invention.

6 Therefore, the Invention and the Cited Invention are identical or different in the following features.

[Corresponding Feature]

"A device used for reading a bar code, the device comprising:

a two-dimensional image sensor array, the two-dimensional image sensor array being made from a complementary metal oxide semiconductor, the two-dimensional image sensor array containing rows of pixels;

an image pickup lens that focuses light on the two-dimensional image sensor array;

an illumination light source used for projecting an illumination pattern, the illumination light source being made from a light-emitting diode; and

a global electronic shutter control module that is disposed so as to simultaneously expose a plurality of rows of pixels of the two-dimensional image sensor array, during an exposure period, the global electronic shutter control module being configured to control the two-dimensional image sensor array so that the exposure of the plurality of rows of pixels in the two-dimensional image sensor array is simultaneously started,

wherein the device is characterized by the exposure period and an illumination period in which the light-emitting diode can be simultaneously driven

during the illumination period, and adjustment between the exposure period and the illumination period is at least partially overlapped in time".

[Different Feature]

The Invention has "a support assembly, the support assembly containing a lens holder for supporting the image pickup lens," whereas it is unclear that the Cited Invention includes a corresponding configuration.

No. 6 Judgment

1 Regarding [Different Feature]

Since an optical reader for reading a bar code picks up an image of a bar code on an image sensor through a lens, it is obvious that the optical reader includes the configuration of retaining the lens. Then, as a specific configuration of retaining the lens of the optical reader for reading a bar code, as "an optical reader for reading a bar code, wherein an imaging module 50 capable of decoding bar code indicia includes a support 80 having a containment 81 containing an image sensor 32 incorporated on a chip 182, and a retainer section 82 retaining a lens assembly 40 provided with one or more lenses provided by a lens barrel" is described in Cited Document 2, it is recognized as a publicly known technology that a lens holder for supporting an image pickup lens and a support assembly containing the lens holder are provided by including "a lens assembly 40" as the one retaining a plurality of lenses, and including "a support 80 having a retainer section 82" as the one containing the lens assembly 40.

Therefore, since the configuration for retaining a lens of "a lens portion 1" is necessary also in the Cited Invention that is "a bar code reading device," making the configuration relating to [Different Feature] is a matter which can be appropriately achieved by a person skilled in the art by adopting the publicly known technology in the matter described in Cited Document 2 as the configuration for retaining.

2 Appellant's allegation

(1) The Appellant, in the written opinion submitted on January 18, 2019, alleges that "4-3-2. Regarding the invalidity of logic of lack of inventive step by the combination of Cited Documents 1 and 2 with respect to Invention 1, the administrative judge points out that other configurations are disclosed except for the configuration relating to 'the support assembly containing a lens holder for supporting the image pickup lens'.

However, we cannot accept the indication of the administrative judge. The reason will be described in detail below.

Cited Document 1 does not disclose at least the configuration relating to 'a global electronic shutter control module that is disposed so as to simultaneously expose a plural rows of pixels of the two-dimensional image sensor array, during an exposure period, the global electronic shutter control module configured to control the two-dimensional image sensor array so that the exposure of the plurality of rows of pixels in the two-dimensional image sensor array is simultaneously started' of Constituent component F of Invention 1.

That is, FIG. 5 of Cited Document 1 and Paragraphs [0020] to [0025] of the specification related to them roughly describe the following (underlines are added).

'[0020] A signal TXa that simultaneously selects the gate of a transfer MOS transistor TX in FIG. 3 for all the pixels from the first row to the mth row is connected to each transfer MOS transistor TX through an OR circuit with transfer pulses TX1 to TXn of the signal that selects all the pixels for each row. Further, in order to simultaneously reset the gates of the amplification MOS transistors M3 of all the pixels, a signal RESa that simultaneously selects the gates of the reset MOS transistors M1 of all the pixels from the first row to the mth row is connected to each reset MOS transistor M1 through an OR circuit with pulses RES1 to RESn that reset the pixels for each row.

[0021] In this image sensor, first, a pulse φRESa to the gate of the reset MOS transistor M1, a gate pulse φTXa of the transfer MOS transistor TX, and the pulse φVRES to the gate of a vertical signal line reset MOS transistor M8 are at high levels. Therefore, the gate of the amplification MOS transistor M3 and the photodiode PD are reset to the voltage VR, and the vertical signal lines V1 to Vn are reset to the voltage VVR (up to t2 in FIG. 5).

[0022] Next, φTXa becomes low level, and the photodiode PD can generate an electric charge according to the light (t2). In the LED lighting mode, the control signal φLED becomes high level and the LED is lit prior to t2 (t1). Subsequently, the pulse φRESa to the gate of the reset MOS transistor M1 and the gate pulse φVRES of the vertical signal line reset MOS transistor M8 become low level, and the reset of the gate of M1 and the vertical signal line is released (t3). After a predetermined time from time t3, φTXa is set to a high level again and the charge of the photodiode PD is transferred to the gate of the amplification MOS transistor M3 (t4).

[0023] After a sufficient time for transfer, the φTXa is lowered again to end the charge transfer of the photodiode PD (t5). In this case, the photoelectric conversion time is between t2 and t5. In the mode in which the LED is turned on, the LED is turned off after the transfer is ended (t6). Next, the gate pulse φSEL1 of the selection MOS transistor M2 and the gate pulse φTS of the optical signal transfer MOS transistor M5

become high levels (t7). Therefore, the optical signal voltage is read out to the optical signal holding capacitance CTS (t7 to t8). After reading to the capacitive CTS, the pulse φRES1 to the gate of the reset MOS transistor M1 and the gate pulse φVRES of the reset MOS transistor M8 become high level, and the gate of M1 and the vertical signal line are reset (t9). Subsequently, φRES1 and φVRES become low level (t10), and after the reset of the gate of M1 and the vertical signal line is released, the gate pulse φSEL1 of the selection MOS transistor M2 and the gate pulse φTN of a noise signal transfer MOS transistor M4 become high level (t11). Therefore, the noise voltage is read out to the optical signal holding capacitance CTN (t11 to t12). After that, the gates of the horizontal transfer switches M6 and M7 in each row are sequentially raised to a high level by the signals H1 to Hn from the horizontal scanning circuit block HSR, and voltage held in the noise holding capacitance CTN and the optical signal holding capacitance CTS is sequentially read out to a differential circuit block (t14 to t15). In the differential circuit block, differences between the optical signal and the noise signal are taken, and are sequentially output to an output terminal VOUT.

[0024] With the above, the reading of the pixel cell connected to the first row is completed. After that, prior to the reading of the second line, φCTR to the gates of the reset switches M9 and M10 of the noise signal holding capacitance CTN and the optical signal holding capacitance CTS becomes high level and are reset to VRCT.

[0025] Similarly, the signals of the pixel cells C21 to Cmn connected to the second row to the mth row are sequentially read out by the signals from the vertical scanning circuit block VSR, and the reading of all the pixel cells is completed.'

The administrative judge points out that the exposure of all pixels is performed during the periods t2 to t5. On the other hand, it is pointed out that only the first row of the pixels is read out during the periods t7 to t15, and then the reading of the second row or later is performed.

However, while the administrative judge recognized that at least the periods t7 to t15 are applied only to the first row of the pixels and no corresponding timing for the 2nd to mth rows of the pixels shown in FIG. 5 is indicated at all, the administrative judge does not explain how to apply the description relating to FIG. 5 to all the pixels in the array (or whether or not it can be said that it is indicated how all the pixels are simultaneously operated).

Therefore, it cannot be said that the indication of the administrative judge that Cited Document 1 performs the exposure operation similar to Invention 1 is reasonable.

As described above, Invention 1 could not have been easily conceived by a

person skilled in the art on the basis of the inventions described in Cited Documents 1 and 2, and does not fall under Article 29(2) of the Patent Act".

(2) Then, the allegation above will be examined.

The Appellant's allegation is summarized that no timing is indicated in FIG. 5 with respect to the second row to the mth row of the pixels, so that the judgment that the Invention performs the similar exposure operation from Cited Document 1 is not reasonable.

However, although the Invention describes "comprising a global electronic shutter control module that is disposed so as to simultaneously expose a plurality of rows of pixels of the two-dimensional image sensor array, during an exposure period, the global electronic shutter control module being configured to control the two-dimensional image sensor array so that the exposure of the plurality of rows of pixels in the two-dimensional image sensor array is simultaneously started," it is not specified how to output the exposed data from each row after the exposure period, so that the Appellant's allegation is not based on the description of the claims.

Further, on the basis of the description "similarly, the signals of the pixel cells C21 to Cmn connected to the second row to the mth row are sequentially read out by the signals from the vertical scanning circuit block VSR, and the reading of all the pixel cells is completed" of Paragraph [0025] of Cited Document 1, it is obvious that the second row to mth row of the pixels are also read out in the same manner as the first row, so that the Appellant's allegation itself is groundless and cannot be accepted.

3 Summary

Therefore, the Invention could have been easily invented by a person skilled in the art on the basis of the invention described in Cited Document 1 and the matter described in Cited Document 2.

No. 7 Closing

As described above, since the Invention could have been easily invented by a person having a usual knowledge in the technical field to which the Invention belongs before the application was filed, on the basis of the invention described in Cited Document 1 and the matter described in Cited Document 2, which had been distributed or available to public over an electric communication network in in Japan or a foreign country before the priority date of the application, the Appellant should not be granted a patent for the Invention under the provisions of Article 29(2) of the Patent Act.

Accordingly, without examining inventions relating to other claims, the present application should be rejected.

Therefore, the appeal decision shall be made as described in the conclusion.

March 4, 2019

Chief administrative judge: IIDA, Kiyoshi
Administrative judge: ODA, Hiroshi
Administrative judge: KAJIO, Seiya