Advisory opinion

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The advisory opinion on the technical scope of a patent invention for Patent No. 4510060 between the parties above is stated and concluded as follows.

Conclusion

A read/write control method of a flash-memory of nonvolatile semiconductor memory indicated in the explanatory document of Article A falls within the technical scope of the invention described in Claim 2 of Patent No. 4510060.

Reason

No. 1 Object of the demand

The object of the advisory opinion is to demand the advisory opinion that a method executed by a flash-memory indicated in the explanatory document of Article A (hereinafter, referred to as "Article A") falls within the technical scope of the invention described in Claim 2 of the scope of claims for patent (hereinafter, referred to as "the patent invention") of Patent No. 4510060 (hereinafter, referred to as the "Patent").

Also, regarding "Article A" in the object of the demand, on Pages 14 to 15 of the written request for the advisory opinion, considering that Article A as a method is compared with the Patent, it does not substantially change the summary of the demand. Also, to the inquiry dated February 13, 2018, the demandant, in the written reply submitted on March 15, 2018 (hereinafter, referred to as "Written reply 1 of the demandant"), corrected "a flash-memory" to "a method executed by a flash-memory," and since there is no change in "MX30UF4G28AB-T1" which is the subject of the

determination regarding Article A, it does not replace or add to the major facts, and thus the determination is made as the object of the demand as described above.

No. 2 Regarding the present invention
1. History of the procedures

Application	September 14, 2007
Publication of the application	April 2, 2009
Request for examination	August 7, 2009
Notice of reasons for refusal	dated January 5, 2010
Written reply and Written amendment	March 15, 2010
Decision to grant a patent	dated April 1, 2010
Registration of establishment of patent right	May 14, 2010
Written request for an advisory opinion	October 11, 2017
Written reply	February 5, 2018
Inquiry (by the body)	dated February 13, 2018
Written refutation (1)	March 15, 2018
Written reply (1) (the demandant)	March 15, 2018
Written refutation (2)	March 19, 2018
Inquiry (by the body)	dated April 10, 2018
Written reply (2) (the demandant)	May 14, 2018
Written reply (the demandee)	June 12, 2018

2. Constitution of the patent invention

According to the description of the scope of claims for patent, the patent invention is as follows. (Note by the body: according to the written request for an advisory opinion "B: the separate description of the constituent components" (Page 4, lines 3 to 20), the invention is separately described in relation to each constituent component, and symbols 2A to 2D are added. Hereinafter, referred to as "the constituent component 2A" and the like.)

"2A and 2D A read/write control method of a nonvolatile semiconductor memory which has a NAND string having a plurality of floating gate nonvolatile memory cells connected in series, and a plurality of word lines connected to control gates of the respective memory cells in the NAND string, wherein

2B when performing write verification and normal reading to selected memory cells in the NAND string by applying selection voltage to selected word lines and applying read pass voltage turning on non-selected memory cells to non-selected word lines regardless of cell data,

2C a first read pass voltage is applied from a drive circuit to the non-selected word lines except for two adjacent non-selected word lines adjacent to the selected word line, and a second read pass voltage which is higher than the first read pass voltage is applied from the drive circuit to the two adjacent non-selected word lines."

3. Descriptions in the specifications of the Patent
(1) In the detailed explanation of the invention of the specification of the Patent, a

problem of the patent invention, a means for solving the problem, and an effect thereof are described as follows. (Note by the body: the underlines were added by the body; the same shall apply hereinafter.)

"[Background Art]
[0002]

In a current NAND flash memory, each memory cell is provided with a floating gate (FG), and performs writing and erasing by the electron-injection and electron-releasing of the FG. By controlling the amount of electron injection in the FG, a plurality of threshold value states (data status) can be set up. In recent years, the NAND flash memory which makes one memory cell memorize 2 bits; i.e., 4 values, is developed and mass-produced.
[0003]

In the miniaturization and the further multi-valuing of the NAND flash memory, interference noise between the floating gates (FG) has been problem. It is an effect that assuming a memory cell Cell_A is written, and then adjacent memory cell Cell_B is written, the FG potential of Cell_A changes in response to the influence of the change of FG potential of Cell_B, and the threshold value distribution seems to be widened as a result.
[0004]

As a preferable write control scheme which decreases an influence of interference between such memory cells, a system of Patent Document 1 is proposed, for example. Here, basically, an upper level page write mode that brings the lowest level of 4 value level straight to the highest level is not used. Thereby, the interference noise between adjacent memory cells can be reduced. Furthermore, for example, word lines are basically selected in order from the source line in the write control scheme, and word line selection orders of the lower page write and the upper page write are suitably combined so as to reduce the interference between the adjacent memory cells as much as possible.
[0005]

However, even if using the write control scheme of the Patent Document 1, when the further miniaturization of the NAND flash memory is advanced, it becomes difficult to avoid the influence of the interference noise between the adjacent cells.
[Patent Document 1] Japanese Unexamined Patent Application Publication No 2005-243205
[Description of the Invention]
[Problem to be solved by the invention]
[0006]

An object of the present invention is to provide the read/write control method of a nonvolatile semiconductor memory which reduces interference noise between adjacent cells.

"[0040]
[Problem to be Solved]

Although the basic constitution and the basic writing control scheme of the NAND flash memory of the embodiment have been explained above, a problem to be solved still remains here. This will be described specifically below.

[0041]

FIG. 5 shows a bias relationship in the NAND string at the time of write verify reading, and normal reading. Here, in order to simplify the description, there is shown an example in which memory cells configuring the NAND string are eight memory cells of MC0 to MC7.

[0042]

When the memory cell MC2 is selected, a selection voltage Vsel is applied to a word line WL2 thereof, and a read pass voltage Vread which is required to turn on the non-selected cells regardless of data states is applied to word lines WL0 to 1 and WL3 to 7 of other non-selected cells MC0 to MC1 and MC3 to MC7. The selection voltage Vsel is, as shown in FIG. 4, any one of the verify voltage VLv Vav, Vbv, and Vcv selected according to a write level at the time of write verification, and is any one of read voltage Var, Vbr, and Vcr set between respective levels selected according to a level at the time of normal reading.

[0043]

FIG. 6 shows a state of the memory cells in a range of word lines WLn-2 to WLn+2 at the time of the write verification in the upper level page writing which writes an A level in the memory cell of the selected word line WLn. When performing the upper level page writing to the memory cell of the word line WLn, all of writing of the memory cells of the word lines WLn-1 to WLn-2 have been completed, and they are set at either one of E-C levels. The memory cell of the word line WLn+1 is in a state in which lower page data (LM level) are written or in the E level, according to a writing order described in FIG. 2. The memory cell of the further adjacent word line WLn+2 is in the E level (erase state).

[0044]

Here, focusing on the C level of the memory cell of the word line WLn-1 already written, if this distribution is not influenced by the interference between the floating gates from the circumference, it has a distribution b1 of a solid line, and if being influenced by the interference, it has a distribution b2 of a broken line. In the word line WLn+1, if there is no interference, it has a distribution c1 of a solid line, and if there is an interference, it has a distribution c2 of a broken line.

[0045]

Here, considering the interference between the adjacent cells, it is noticed that the non-selected word lines WLn-1 and WLn+1 adjacent to the selected word line WLn have different conditions from other non-selected word lines. That is, other non-selected word lines and the selected word lines are sandwiched by the word lines to which Vread is applied, whereas, in word lines WLn+1 and WLn-1, one of the word lines at both ends thereof is at Vread and the other is at the verify voltage Vav.

[0046]

Thereby, regarding the memory cells of the non-selected word lines WLn-1 and WLn+1 with which the electric potential of one of the adjacent word lines is low, as compared with the cells of other non-selected word lines, the interference of the adjacent cell is large, and an apparent threshold value becomes high. This will be more specifically described with reference to FIG. 8.

[0047]

FIG. 8 shows a situation of capacitive coupling which affects the electric potential while focusing on the floating gate FGn of the memory cell MCn in the

NAND string. That is, the FGn is coupled with a control gate (namely, the word line WLn) thereabove via capacitance C2, and is coupled with a channel via capacitance C1. Basically, floating gate potential and channel potential are controlled by the word lines at the coupling ratio of these capacitances C2 and C1.

[0048]

On the other hand, due to the miniaturization of the cell, the floating gate FGn of the cell of interest is strongly coupled to the floating gates of the adjacent cells and the word lines of the adjacent cells with the capacitances C3 and C4, respectively.

[0049]

Under such capacitive coupling situation, considering the floating gate FGn+1 under the word line WLn+1 when pass voltage Vread is applied to the word line WLn+1 and further lower read voltage is applied to the word line WLn, the floating gate FGn+1 becomes lower in potential than the case where FGn+1 is directly controlled by the word line WLn+1 with Vread applied. Because a first capacitive coupling effect that pulls down the electric potential of FGn+1 from the word line WLn via FGn (namely, via the capacitances C2 and C3) and a second capacitance coupling effect that pulls down the electric potential of FGn+1 of the adjacent cell from the word line WLn directly (namely, an effect which pulls down the electric potential of FGn+1 via the capacitance C4) are overlapped, in the floating gate FGn+1, an electric potential rise due to Vread is not sufficiently performed.

[0050]

In other words, in the memory cell under a non-selected word line adjacent to the selected word line, an apparent threshold value becomes high. Namely, as shown in FIG. 6, the memory cell set at LM level under the non-selected word line WLn+1, has apparent distribution “c3” shown by a dashed line while the memory cell set at C level under the non-selected word line WLn-1 has distribution “b3” shown by a dashed line.

[0051]

As a result, as shown in FIG. 6, a relationship between an on-margin dVon_2a against Vread of a cell under the non-selected word line WLn-1 and an on-margin dVon_1a against Vread of another cell under the non-selected word line WLn-2 becomes dVon_1a > dVon_2a.

[0052]

Next, FIG. 7 shows cell threshold value states within the word lines WLn-2 to WLn+2, in a case that the cell data (A level) of the word line WLn is read out after writing all memory cells. Here is shown that all memory cells have threshold distributions shifted in the positive direction (shown by dotted lines) from the predetermined threshold states (shown by solid lines) due to the interference of adjacent cells.

[0053]

Also, in the C level cell under the word line WLn-1, if the read voltage of the selected word line WLn is set at about A level, the same as in the case shown in FIG. 6, it is considered to have the distribution “b3” shown by the dashed line. On the other hand, the C level cell under the word line WLn+1 appears to have the distribution “c3” shown by the dashed line, due to the interference from the cell on the selected word line WLn side to which the read voltage is applied.

[0054]

Threshold value change in the A level cell under the selected word line WLn is

explained as follows. First, since the distributions “c1” to “c3” of the LM level of the cell under WLn+1 in FIG. 6 are shifted to the distributions “c1” to “c3” of the C level of the cell under WLn+1 in FIG. 7, data distribution “a1” shown by a solid line is shifted to distribution “a2” shown by a dotted line, due to an interference effect between floating gates FG. In addition, the threshold value distribution of the memory cell under the non-selected word line WLn+1 apparently becomes “c3”, and if an increase in ON resistance affects a cell current Icell at the time of setting the threshold value of the memory cell under the selected word line WLn, the data distribution of the memory cell written into the A level under the selected word line WLn further shifts the threshold value in the positive direction as shown by “a3”.

[0055]

Such an effect that the on-margin against the pass voltage Vread of the non-selected cells becomes a cause to expand the data threshold value distribution after writing is referred to as a “back pattern noise”. Generally, this back pattern noise is easier to be seen in the memory cell that is written earlier in the NAND string; that is, the memory cell closer to the cell source line CELSRC side. However, when interference between memory cells increases due to miniaturization, even the influence of one adjacent memory cell cannot be ignored, and influence may be seen by the on-margin which becomes small."

"[0061]

[A R/W method of an embodiment (Part 1)]

FIG. 9 shows an applied voltage state to the word lines in the NAND string during write verify action and normal reading action of a read/write (R/W) method (Part 1) of an embodiment, corresponding to FIG. 5. Also, FIG. 10 shows cell threshold value states of the adjacent word lines during the upper level page write verify action of the selected word line WLn, and FIG. 11 shows the cell threshold value state at the time of reading the selected word line WLn after writing all cells, corresponding to those shown in FIG. 6 and FIG. 7, respectively.

[0062]

As shown in FIG. 9, FIG. 10, and FIG. 11, to the non-selected word line WLn+1 adjacent to the selected word line WLn (on a bit line side; namely on the cell side written after the selected cell), a read pass voltage Vread2 which is higher than the read pass voltage Vread applied to other non-selected word lines is applied to perform the write verification and positive reading action.

...(Omitted)...

[0070]

By introducing such read pass voltage Vread2, an ON resistance rise in the cell under the non-selected word line WLn+1 is suppressed, and thus a threshold value distribution shift of the selected memory cell under the selected word line WLn is suppressed. More specifically, if the ON resistance of the cell under the non-selected word line WLn+1 rises, as described above in FIG. 7, the data distribution of the memory cell written in the A level of the selected word line WLn shifts a threshold value in the positive direction as shown by distribution “a3”.

[0071]

Against this, according to this embodiment, as shown in FIG. 11, shift amount from the data distribution a2 to a3 of the selected memory cell is reduced. Based on

the analysis results described above, this effect becomes remarkable especially in generations with a design rule of 56 nm or less."

"[0072]

[A R/W method of an embodiment (Part 2)]

FIG. 13 shows an applied voltage state to the word lines in the NAND string during write verify action and normal reading action of a read/write (R/W) method (Part 2) of an embodiment, corresponding to FIG. 5 and FIG. 9. Also, FIG. 14 shows cell threshold value states of the adjacent word lines during the upper level page write verify action of the selected word line WLn, and FIG. 15 shows cell threshold value state at the time of reading the selected word line WLn after writing all cells, respectively corresponding to those shown in FIG. 6 and FIG. 10, and FIG. 6 and FIG. 11.

[0073]

The difference between the R/W method (Part 2) and the R/W method (Part 1) mentioned before, as shown in FIG. 13, is that at the time of write verify reading, and normal reading, not only to the adjacent non-selected word line WLn+1 on the bit line side of the selected word line WLn, but also to the adjacent non-selected word line WLn-1 on the source line side, the read pass voltage Vread2 which is higher than the read pass voltage Vread applied to other non-selected word lines is applied.

[0074]

Also in this case, Vread2 is a voltage which is adjusted to the extent of cancelling an apparent threshold value increase of the non-selected cells on the adjacent non-selected word lines WLn+1 and WLn-1 due to the read voltage of the selected word line WLn.

If Vread2-Vread is set too large, the on-margin against Vread is reduced in a non-selected word line in which both sides are Vread as side effects, and the back pattern noise due to word lines WLn+2 to WLm tends to increase. Therefore, it is desirable to set Vread2 to the extent that the influence on the memory cell under word line WLn + 1 is suppressed.

[0075]

According to such a R/W method (Part 2), in addition to the effect of the previous R/W method (Part 1), a cell current Icell of the whole of the NAND string at the time of write verification and normal reading due to the lowering of the on-margin in the cell of WLn-1 is suppressed."

(2) From (1) above, it can be recognized as follows.

A Regarding the problem to be solved by the patent invention

(A) In the miniaturization and the further multi-valuing of the NAND flash memory, interference noise between the floating gates (FG) has been problem, and it is an effect that assuming a memory cell Cell_A is written, and then adjacent memory cell Cell_B is writeen, the FG potential of Cell_A changes in response to the influence of the change of FG potential of Cell_B, and the threshold value distribution seems to be widened as a result. (Paragraph [0003])

(B) As a preferable write control scheme which decreases an influence of interference between such memory cells, although a system which does not use an upper level page

write mode that brings the lowest level of 4 value level straight to the highest level is proposed, even if using such a write control scheme, when the further miniaturization of the NAND flash memory is advanced, it becomes difficult to avoid the influence of the interference noise between the adjacent cells. (Paragraphs [0004] to [0005])

(C) Specifically, in an example in which memory cells configuring the NAND string shown in FIG. 5 are eight memory cells of MC0 to MC7, when the memory cell MC2 is selected, although selection voltage Vsel is applied to a word line WL2 thereof, and read pass voltage Vread which is required to turn on the non-selected cells regardless of data states is applied to word lines WL0 to 1 and WL3 to 7 of other non-selected cells MC0 to MC1 and MC3 to MC7, regarding the non-selected word lines WLn-1 and WLn+1 adjacent to the selected word line WLn, since the electric potential of the selected word line WLn which is an adjacent word line is low, as compared with the cells of other non-selected word lines, the interference of the adjacent cell is large, and an apparent threshold value becomes high. As a result, a relationship between an on-margin dVon_2a against Vread of a cell under the non-selected word line WLn-1 and an on-margin dVon_1a against Vread of another cell under the non-selected word line WLn-2 becomes dVon_1a > dVon_2a. (Paragraphs [0041], [0042], [0045], [0046], and [0051])

Such an effect that the on-margin against the pass voltage Vread of the non-selected cells becomes a cause to expand the data threshold value distribution after writing is referred to as a “back pattern noise”, and when interference between memory cells increases due to miniaturization, even the influence of one adjacent memory cell cannot be ignored, and influence may be seen by the on-margin which becomes small. (Paragraph [0055])

B Regarding a means for solving a problem in the patent invention

For the purpose of solving the above-mentioned problem in the prior art, at the time of write verify reading, and normal reading, not only to the adjacent non-selected word line WLn+1 on the bit line side of the selected word line WLn, but also to the adjacent non-selected word line WLn-1 on the source line side, the read pass voltage Vread2 which is higher than the read pass voltage Vread applied to other non-selected word lines is applied. (Paragraph [0073])

C Regarding an effect by the patent invention

By adopting the above mentioned constitution, there can be exerted the effects that an ON resistance rise in the cells under the non-selected word lines WLn-1 and WLn+1 is suppressed, thus a threshold value distribution shift of the selected memory cell under the selected word line WLn is suppressed, and a cell current Icell of the whole of the NAND string at the time of write verification and normal reading due to the lowering of the on-margin in the cell of WLn-1 is suppressed. (Paragraphs [0070] and [0075])

Also, at that time, Vread2 applied to the non-selected word lines WLn-1 and WLn+1 is a voltage which is adjusted to the extent of cancelling an apparent threshold value increase of the non-selected cells on the adjacent non-selected word lines WLn+1

and WLn-1 due to the read voltage of the selected word line WLn (Paragraph [0074]);

that is, so as to exert the above mentioned effect which suppresses the ON resistance rise in the cells under the non-selected word lines WLn-1 and WLn+1, it is acknowledged that to the non-selected word lines WLn-1 and WLn+1 which are adjacent to the selected word line WLn and in which the interference between the memory cells with that is a problem, Vread2 which is a voltage adjusted to the extent of cancelling an apparent threshold value increase of the non-selected cell is applied, and to other non-selected word lines which are not influenced by the selected word line WLn having a lower electric potential, as described in B above, Vread (< Vread2) is applied. (Paragraph [0073])

No. 3 Specification of Article A

1. A flash-memory executing Article A
(1) Specification by the collegial body
A Regarding a flash-memory executing Article A, although the explanatory document of Article A submitted with the written request for the advisory opinion dated October 11, 2017 describes that

'Article A is a flash-memory whose product number is "MX30UF4G28AB-T1" (Evidence A No. 2, Pages 4 and 5)' (the explanatory document of Article A, Page 1, Lines 2 to 3),

According to Evidence A No. 4 (an affidavit (Eiichi MAKINO)) submitted with Written reply 1 of the demandant (hereinafter, referred to as Evidence A No. 4), on November 25, 2016, Eiichi MAKINO, who is an employee of Toshiba Memory Corporation, decided to carry out a needle contact analysis of "MX30UF4G28AB-T1" in response to a request from Takashi ISHIKAWA of the Intellectual Property Department of Toshiba Electronic Devices & Storage Corporation (Page 2 of Evidence A No. 4, Attachment ●2 ("●2" indicates a circled number of "2"; the same shall apply hereinafter)), instructed the needle contact analysis to Yuka FURUTA, who is an employee of Toshiba Memory Corporation, on November 30, 2016 (Page 5 of Evidence A No. 4, Attachment ●2), received two pieces of "MX30UF4G28AB-T1" from ELE TECH Inc. on December 1, 2016 (Page 4 of Evidence A No. 4, Attachment ●2), and received the submission of a material summarizing measurement results (Attachment ●12 of Evidence A No. 4) by the needle contact of "MX30UF4G28AB-T1" (Page 7 of Evidence A No. 4, Attachment ●13) from Yuka FUKUTA on December 12, 2016. Considering that the material summarizing measurement results (Attachment ●12 of Evidence A No. 4) is the source material of Evidence A No. 2 (an investigation report), it can admitted without contradiction that "MX30UF4G28AB-T1" was actually targeted for analysis in Evidence A No. 2.

From the above, as Article A, a method executed in the flash-memory of the product number "MX30UF4G28AB-T1" can be specified.

B Also, since the analysis result of a reading action to the flash-memory of A above is indicated on Pages 9 to 13 of Evidence A No. 2 and the analysis result of a writing action to the flash-memory is indicated on Pages 14 to 19 of Evidence A No. 2, a

read/write control method of a flash-memory is acknowledged as a method executed in the flash-memory of "MX30UF4G28AB-T1".

C Also, according to Pages 8 and 16 of Evidence A No. 3 (a data sheet of "MX30UFxG26(28)AB"), it can be specified that the flash-memory of A above is a NAND flash memory and has a NAND string having 32 cells connected in series, and it is self-evident that each cell configuring the NAND flash-memory is a nonvolatile memory cell having a floating gate and a control gate and that each word line is respectively connected to the control gate of each cell.

D As described above, according to A to C above, as Article A,

a read/write control method of a NAND flash-memory of a product number "MX30UF4G28AB-T1" which has a NAND string having 32 floating gate nonvolatile memory cells connected in series, and a plurality of word lines connected to control gates of the respective memory cells in the NAND string can be specified and recognized.

(2) The demandee's allegation

Against that, although the demandee, in a written reply dated February 5, 2018 (hereinafter, referred to as "the written reply"), alleges

'Even if seeing Evidence A No. 2 (hereinafter, referred to as "Evidence A No. 2", an investigation report), there is no evidence indicating that the flash-memory targeted for verification is "MX30UF4G28AB-T1". Although on Page 5 of Evidence A No. 2, a very unclear photo is posted (furthermore, it seems to be a copy of another report from the description of "Report No. J1FAA11314" on the upper right), the product number cannot be specified from a package photo of the element.' (Page 4, Lines 7 to 12 of the written reply)

'This point is the same even if looking at the photo posted on Page 1 of the explanatory document of Article A. Although the photo posted on the same page is as follows, from this photo, as characters related to the product number, "MX30UF" and "-T1" can be read, but it is impossible to read what the characters described between them are.

...(Omitted)...

Although the explanatory document of Article A should be created based on evidence, such an explanation of Product A which is not based on evidence is groundless and inappropriate.'
(Pages 5, Lines 3 to 12 of the written reply),

since it can admitted without contradiction that "MX30UF4G28AB-T1" was actually targeted for analysis in Evidence A No. 2 from a series of circumstances indicated in Evidence A No. 4, the allegation of the demandee discussed above cannot be accepted.

2. Regarding reading/writing of Article A

(1) Specification by the collegial body

A Regarding the reading/writing of Article A, the explanatory document describes as follows.

(A) The page reading action of "MX30UF4G28AB-T1" will be described. According to an ac waveform of the data sheet of "MX30UF4G28AB-T1 (Evidence A No. 3, Page 19), a reading action is performed by issuing a command of "00h", designating each address, and issuing a command of "30h". (Page 5, Line 1 to Page 7, Line 6 of the explanatory document of Article A)

(B) The page writing action of "MX30UF4G28AB-T1" will be described. According to an ac waveform of the data sheet of "MX30UF4G28AB-T1 (Evidence A No. 3, Page 28), a writing action is performed by issuing a command of "80h", designating each address, and issuing a command of "10h". (Page 10, Line 10 to Page 11, the last line of the explanatory document of Article A)

Also, on Pages 9 to 13 and Pages 14 to 19 of Evidence A No. 2, the analysis results of the reading action and write verify action to the flash-memory according to Article A are respectively indicated, and it can be said to be a matter of technical common sense that when performing read/write verification to a NAND flash-memory, selection voltage for reading/writing is applied to word lines connected to control gates of memory cells to be read/written in a NAND string, and read pass voltage for turning on the memory cells is applied to word lines connected to memory cells except for the memory cells to be read/written in the NAND string respectively, it can be recognized that

the method of Article A specified in 1. (1) D above is a method in which when performing write verification and reading by designating addresses and issuing commands to memory cells to be read/written in the NAND string, selection voltage for reading/writing is applied to word lines connected to control gates of the memory cells to be read/written in the NAND string, and read pass voltage for turning on the memory cells is applied to word lines connected to control gates of memory cells except for the memory cells to be read/written in the NAND string.

3. Regarding voltage at the time of reading/writing by Article A
(1) Specification by the collegial body
A According to Page 15 of Evidence A No. 3, it can be recognized that the NAND flash-memory related to Article A specified in 1. (1) D has a high voltage circuit.

B Also, according to the analysis result shown in the waveform diagrams on Pages 11 to 12 of Evidence A No. 2, it can be recognized that in the reading of the NAND flash-memory related to Article A, when the values of addresses of memory cells to be read are incremented one by one, if measuring voltage about each word line of a word line 1, a word line 20, and a word line 26, in the case that the word line is addressed so as to be a word line of the memory cells to be read, the measurement voltage is 0.48 V, and in the case that it is addressed so as to be a word line adjacent to the word lines of the memory cells to be read, the measurement voltage is 6.4 V, and in the case that it is addressed so as to be a word line except for the word lines of the memory cells to be

read and the word lines adjacent to the word lines of the memory cells to be read, the measurement voltage is 5.9 V.

C Also, according to the analysis result shown in the waveform diagram on Page 13 of Evidence A No. 2, it can be recognized that in the reading of the NAND flash-memory related to Article A, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be read, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.9 V, the measurement voltage of the word line 24 is 6.4 V, the measurement voltage of the word line 25 is 0.48 V, the measurement voltage of the word line 26 is 6.4 V, and the measurement voltage of the word line 27 is 5.9 V.

D Also, according to the analysis result shown in the waveform diagrams on Pages 16 to 18 of Evidence A No. 2, it can be recognized that in the write verification of the NAND flash-memory related to Article A, when the values of addresses of memory cells to be written are incremented one by one, if measuring voltage about each word line of a word line 1, a word line 20, and a word line 26, in the case that the word line is addressed so as to be a word line of the memory cells to be written, the measurement voltage is 2.0 V, and in the case that the word line is addressed so as to be a word line adjacent to the word lines of the memory cells to be written, the measurement voltage is 6.2 V, and in the case that the word line is addressed so as to be a word line except for the word lines of the memory cells to be written and the word lines adjacent to the word lines of the memory cells to be written, the measurement voltage is 5.7 V.

E Also, according to the analysis result shown in the waveform diagram on Page 19 of Evidence A No. 2, it can be recognized that in the write verification of the NAND flash-memory related to Article A, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be written, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.7 V, the measurement voltage of the word line 24 is 6.2 V, the measurement voltage of the word line 25 is 2.0 V, the measurement voltage of the word line 26 is 6.2 V, and the measurement voltage of the word line 27 is 5.7 V.

F As described above, according to A to E, it can be recognized that in Article A,

the NAND flash-memory has a high voltage circuit;

in the reading of the NAND flash-memory, when the values of addresses of memory cells to be read are incremented one by one, if measuring voltage about each word line of a word line 1, a word line 20, and a word line 26, in the case that the word line is addressed so as to be a word line of the memory cells to be read, the measurement voltage is 0.48 V, and in the case that it is addressed so as to be a word line adjacent to the word lines of the memory cells to be read, the measurement voltage is 6.4 V, and in the case that it is addressed so as to be a word line except for the word lines of the memory cells to be read and the word lines adjacent to the word lines of the memory cells to be read, the measurement voltage is 5.9 V;

in the reading of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be read, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.9 V, the measurement voltage of the word line 24 is 6.4 V, the measurement voltage of the word line 25 is 0.48 V, the measurement voltage of the word line 26 is 6.4 V, and the measurement voltage of the word line 27 is 5.9 V;

in the write verification of the NAND flash-memory, when the values of addresses of memory cells to be written are incremented one by one, if measuring voltage about each word line of a word line 1, a word line 20, and a word line 26, in the case that the word line is addressed so as to be a word line of the memory cells to be written, the measurement voltage is 2.0 V, and in the case that the word line is addressed so as to be a word line adjacent to the word lines of the memory cells to be written, the measurement voltage is 6.2 V, and in the case that the word line is addressed so as to be a word line except for the word lines of the memory cells to be written and the word lines adjacent to the word lines of the memory cells to be written, the measurement voltage is 5.7 V; and

in the write verification of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be written, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.7 V, the measurement voltage of the word line 24 is 6.2 V, the measurement voltage of the word line 25 is 2.0 V, the measurement voltage of the word line 26 is 6.2 V, and the measurement voltage of the word line 27 is 5.7 V.

(2) The demandee's allegation

Against that, although the demandee, in the written reply, alleges that

"On Page 6 of Evidence A No. 2, as an explanation of a photo, only a number such as 'CG●●' is indicated, and in the first place, it is not shown at all that a line indicating the number corresponds to a word line. Also, it cannot be understood what the number such as 'CG25' itself is based on." (Page 6, third line from the bottom to Page 7, Line 1 of the written reply),

since it is recognized that a connection relationship between a word line of a polysilicon wiring layer of "MX30UF4G28AB-T1" which is the NAND flash-memory related to Article A and a CG line of a third wiring layer can be confirmed by peeling and analyzing each wiring layer, and connection relationships between the CG lines (CG0 to CG31) and WordLine (WL0 to WL31) are indicated on Page 3 of Attachment ●4 of Evidence A No. 7 (a semiconductor product analysis report dated March 7, 2018), it can be recognized that all word lines are connected to any one of the CG lines, and a waveform of the corresponding word line can be observed by measuring the waveform of the CG line. Therefore, since it can be recognized that the investigation related to Evidence A No. 2 was performed by confirming to which CG line each word line of "MX30UF4G28AB-T1" which is the NAND flash-memory related to Article A is connected, the allegation of the demandee discussed above cannot be accepted.

4. Article A

In the summary of 1. to 3. above, it is recognized that Article A is equipped with components separately described as follows (codes 2a-2d are assigned to each component; hereinafter, the separately described components are referred to as "a component 2a" and the like.).

"2a and 2d A read/write control method of a NAND flash-memory of a product number 'MX30UF4G28AB-T1' which has a NAND string having 32 floating gate nonvolatile memory cells connected in series, and a plurality of word lines connected to control gates of the respective memory cells in the NAND string, wherein

2b when performing write verification and reading by designating addresses and issuing commands to memory cells to be read/written in the NAND string, selection voltage for reading/writing is applied to word lines connected to control gates of the memory cells to be read/written in the NAND string, and read pass voltage for turning on the memory cells is applied to word lines connected to control gates of memory cells except for the memory cells to be read/written in the NAND string, and

2c the NAND flash-memory has a high voltage circuit;

in the reading of the NAND flash-memory, when the values of addresses of memory cells to be read are incremented one by one, if measuring voltage about each word line of a word line 1, a word line 20, and a word line 26, in the case that the word line is addressed so as to be a word line of the memory cells to be read, the measurement voltage is 0.48 V, and in the case that it is addressed so as to be a word line adjacent to the word lines of the memory cells to be read, the measurement voltage is 6.4 V, and in the case that it is addressed so as to be a word line except for the word lines of the memory cells to be read and the word lines adjacent to the word lines of the memory cells to be read, the measurement voltage is 5.9 V;

in the reading of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be read, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.9 V, the measurement voltage of the word line 24 is 6.4 V, the measurement voltage of the word line 25 is 0.48 V, the measurement voltage of the word line 26 is 6.4 V, and the measurement voltage of the word line 27 is 5.9 V;

in the write verification of the NAND flash-memory, when the values of addresses of memory cells to be written are incremented one by one, if measuring voltage about each word line of a word line 1, a word line 20, and a word line 26, in the case that the word line is addressed so as to be a word line of the memory cells to be written, the measurement voltage is 2.0 V, and in the case that the word line is addressed so as to be a word line adjacent to the word lines of the memory cells to be written, the measurement voltage is 6.2 V, and in the case that the word line is addressed so as to be a word line except for the word lines of the memory cells to be written and the word lines adjacent to the word lines of the memory cells to be written, the measurement voltage is 5.7 V; and

in the write verification of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be written, if

measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.7 V, the measurement voltage of the word line 24 is 6.2 V, the measurement voltage of the word line 25 is 2.0 V, the measurement voltage of the word line 26 is 6.2 V, and the measurement voltage of the word line 27 is 5.7 V."

No. 4 Judgment of belongingness

Whether or not Article A satisfies constituent components 2A to 2D of the patent invention will be examined.

1. Regarding constituent components 2A and 2D

"Floating gate nonvolatile memory cells," "a NAND string," "control gates," "word lines," and "a NAND flash-memory of 'MX30UF4G28AB-T1'" of the component 2a of Article A respectively correspond to "floating gate nonvolatile memory cells," "a NAND string," "control gates," "word lines," and "a nonvolatile semiconductor memory" of the patent invention, and thus the component 2a of Article A and the constituent component 2A of the patent invention are identical.

Similarly, the component 2d of Article A and the constituent component 2D of the patent invention are identical.

Therefore, the components 2a and 2d of Article A respectively satisfy the constituent components 2A and 2D of the patent invention.

2. Regarding the constituent component 2B

"Word lines connected to control gates of the memory cells to be read/written in the NAND string" and "word lines connected to control gates of memory cells except for the memory cells to be read/written in the NAND string" of the component 2b of Article A respectively correspond to "selected word lines" and "non-selected word lines" of the patent invention, and "selection voltage for reading/writing" applied to "word lines connected to control gates of the memory cells to be read/written in the NAND string" and "read pass voltage for turning on the memory cells" applied to "word lines connected to control gates of memory cells except for the memory cells to be read/written in the NAND string" of the component 2b of Article A respectively correspond to "selection voltage" applied to "selected word lines" and "pass voltage turning on non-selected memory cells" applied to "non-selected word lines" "regardless of cell data" of the patent invention.

Then, it can be said that "when performing write verification and reading by designating addresses and issuing commands to memory cells to be read/written in the NAND string" by applying selection voltage for reading/writing to word lines connected to control gates of the memory cells to be read/written in the NAND string, and applying read pass voltage for turning on the memory cells to word lines connected to control gates of memory cells except for the memory cells to be read/written in the NAND string" related to the component 2b of Article A is identical to "when performing write verification and normal reading to selected memory cells in the NAND string by applying selection voltage to selected word lines and applying read pass voltage turning on non-selected memory cells to non-selected word lines regardless

of cell data" related to the constituent component 2B of the patent invention.

Therefore, the component 2b of Article A satisfies the constituent component 2B of the patent invention.

3. Regarding the constituent component 2C
(1) Judgment

A It can be said that "a word line 25" "when a memory cell of the word line 25 of five continuous word lines 23 to 27" "is selected" "to be read or written" of the component 2c of Article A is "word lines connected to control gates of the memory cells to be read/written in the NAND string" of the component 2b, and thus corresponds to "selected word lines" of the patent invention. Also, "the word line 24" and "the word line 26" "when a memory cell of a word line 25 of five continuous word lines 23 to 27 is selected to be read" of the component 2c of Article A correspond to "two adjacent non-selected word lines adjacent to the selected word line" of the patent invention. Furthermore, in addition to "the word line 23" and "the word line 27" "when a memory cell of a word line 25 of five continuous word lines 23 to 27 is selected to be read" of the component 2c of Article A, it can also be said that word lines except for the "five continuous word lines 23 to 27; namely, "word lines 0 to 22 and 28 to 31," in "a NAND string having 32 floating gate nonvolatile memory cells connected in series" configuring "the NAND flash-memory" related to Article A, correspond to "the non-selected word lines except for two adjacent non-selected word lines adjacent to the selected word line," "when a memory cell of a word line 25 of five continuous word lines 23 to 27 is selected to be read," and thus it can be said that "the word line 23," "the word line 27," and "word lines 0 to 22 and 28 to 31" "when a memory cell of a word line 25 of is selected to be read" of Article A correspond to "the non-selected word lines except for two adjacent non-selected word lines adjacent to the selected word line" of the patent invention.

Also, "6.4 V" or "6.2 V" which is the measurement voltage of "the word line 24" and "the word line 26" and "5.9 V" or "5.7 V" which is the measurement voltage of "the word line 23" and "the word line 27" "when a memory cell of the word line 25 of five continuous word lines 23 to 27" "is selected" to be "word lines to be read or written" of the component 2c of Article A, respectively correspond to "second read pass voltage" and "first read pass voltage" of the patent invention. Since "6.4 V" or "6.2 V" which is the measurement voltage of "the word line 24" and "the word line 26" of the component 2c of Article A has a higher value than "5.9 V" or "5.7 V" which is the measurement voltage of "the word line 23" and "the word line 27," "6.4 V" or "6.2 V" which is the measurement voltage of "the word line 24" and "the word line 26" of the component 2c of Article A corresponds to "second read pass voltage which is higher than the first read pass voltage" of the patent invention. Also, since "5.9 V" or "5.7 V" which is the measurement voltage of "the word line 23" and "the word line 27" of the component 2c of Article A corresponds to "first read pass voltage" of the patent invention and it is reasonable to understand that the measurement voltage of "the word lines 0 to 22 and 28 to 31" of Article A can be measured in the same manner as "the word line 23" and "the word line 27," it can also be said that the measurement voltage of "the word lines 0 to 22 and 28 to 31" corresponds to "first read pass voltage" of the patent invention.

B Here, in Article A, "the NAND flash-memory has a high voltage circuit" as described in the component 2c, and in the investigation method relate to Evidence A No. 2, as "6.4 V" or "6.2 V" measured from "the word line 24" and "the word line 26," and "5.9 V" or "5.7 V" measured from "the word line 23" and "the word line 27" are not supposed to be caused by factors except for voltage application from "a high voltage circuit," it is recognized that it is reasonable to understand that it is caused by the voltage application from "a high voltage circuit." Therefore, it can be said that "a high voltage circuit" of the component 2c of Article corresponds to "a drive circuit" of the patent invention. Also, considering the examination of A above, the fact that "6.4 V" or "6.2 V" measured from "the word line 24" and "the word line 26" of the component 2c of Article A is caused by voltage application from "a high voltage circuit" and the fact that "5.9 V" or "5.7 V" which is the measurement voltage from "the word line 23," "the word line 27," and "the word lines 0 to 22 and 28 to 31" is caused by voltage application from "a high voltage circuit" of the component 2c of Article A respectively correspond to the fact that "second read pass voltage which is higher than the first read pass voltage is applied from the drive circuit to the two adjacent non-selected word lines" and the fact that "first read pass voltage is applied from a drive circuit to the non-selected word lines except for two adjacent non-selected word lines adjacent to the selected word line" of the patent invention.

C Then, it can be said that the facts that "the NAND flash-memory has a high voltage circuit;" "in the reading of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be read, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.9 V, the measurement voltage of the word line 24 is 6.4 V, the measurement voltage of the word line 25 is 0.48 V, the measurement voltage of the word line 26 is 6.4 V, and the measurement voltage of the word line 27 is 5.9 V"; "in the write verification of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be written, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.7 V, the measurement voltage of the word line 24 is 6.2 V, the measurement voltage of the word line 25 is 2.0 V, the measurement voltage of the word line 26 is 6.2 V, and the measurement voltage of the word line 27 is 5.7 V"; and "having 32 floating gate nonvolatile memory cells connected in series" configuring "the NAND flash-memory" related to the component 2c of Article A, are identical to the fact that "first read pass voltage is applied from a drive circuit to the non-selected word lines except for two adjacent non-selected word lines adjacent to the selected word line, and second read pass voltage which is higher than the first read pass voltage is applied from the drive circuit to the two adjacent non-selected word lines" related to the constituent component 2C of the patent invention.

(2) The demandee's allegation

A The demandee, in the written reply submitted on June 12, 2018 (hereinafter, referred to as "the written reply of the demandee") alleges, in summary, as follows.

(A) Since the demandant merely shows the measurement results of CG 23 and CG 27 for "non-selected word lines which are not adjacent non-selected word lines," and indicates no evidence about other "non-selected word lines which are not adjacent non-selected word lines," it can be said that the demandant does not prove the sufficiency of the constituent component 2C. (Page 4, Lines 12 to 21 of the written reply of the demandee)

(B) In the prosecution history of the Patent, the applicant (TOSHIBA CORPORATION which is the parent company of the demandant) alleges as follows about Cited Document 1 (Evidence B No. 3), in the written opinion (Evidence B No. 4) dated March 15, 2010 (date of acceptance), and clearly explains that the rise of the second read pass voltage sometimes does not depend on the application of voltage from the drive circuit,

"Although the one disclosed in Cited Document 1, at a glance, seems to apply first read pass voltage (Vread) to a non-selected word line (CGn) except for two adjacent non-selected word lines adjacent to a selected word line, and apply second read pass voltage (Vread') which is higher than the first read pass voltage to the two adjacent non-selected word lines (CGi-1 and CGi+1) as a reading action of a NAND nonvolatile semiconductor memory, as it is clear from the explanations of Paragraphs [0075] and [0078], when a selected word line WLi rises from Vsel1 to Vsel2, as a result that non-selected word lines WLi-1 and WLi + 1 adjacent to a selected word line WLi come to be in a floating state, the voltage of the adjacent non-selected word lines WLi-1 and WLi+1 is merely raised to the second read pass voltage (Vread') due to an influence of the voltage Vsel2, so that the read pass voltage (Vread') is not applied from a drive circuit, and no voltage is applied from the drive circuit at all."
(Evidence B No. 4, Page 2)

Then, as the applicant of the Patent who is a person skilled in the art explains as described above, it is obvious that it cannot be said that a factor causing a voltage rise (a difference between second voltage and first voltage) at the adjacent non-selected word lines of the selected word line can be other than the voltage application by the high voltage circuit. (Page 5, Line 8 to Page 6, Line 5 of the written reply of the demandee)

B However, none of the demandee's allegation of A above is acceptable, for the following reasons.

(A) Regarding the allegation of A (A) above

a Since it is understood that "the non-selected word lines except for two adjacent non-selected word lines adjacent to the selected word line" in the patent invention indicate all non-selected word lines except for the two adjacent non-selected word lines adjacent to the selected word line from non-selected word lines of word lines respectively connected to control gates of memory cells configuring one NAND string, although the fact that "second read pass voltage" of "the two non-selected word lines" is "higher" than "the first read pass voltage" of "the non-selected word lines except for two adjacent non-selected word lines adjacent to the selected word line" means that "the first read pass voltage" lower than the "second read pass voltage" is applied to all "non-selected word lines except for the two adjacent non-selected word lines adjacent to the selected word line" among the non-selected word lines connected to the memory cells

configuring one NAND string, Evidence A No. 2 does not show all measurement results (of the word lines 0 to 23 and 27 to 31, only measurement results of the word lines 23 and 27 are shown) of what kind of voltage is applied to the non-selected word lines except for the two adjacent non-selected word lines adjacent to the selected word line, when a certain word line is addressed so as to be read/written ("the word line 25" in the component 2c of Article A), about Article A.

b However, since in Article A, as described in the component 2c, "the NAND flash-memory has a high voltage circuit," and it is understood that an address is designated by a common address circuit to select a line about all of the CG lines 0 to 31 corresponding to the word lines 0 to 31, when designating the values of addresses of the memory cells to be read/written, if measuring voltages about the word lines 0 to 31, it can be understood that the same voltage as the other word lines can be measured in each state of a state addressed so as to be the word line of the memory cells to be read/written, a state addressed so as to be the word lines adjacent to the word line of the memory cells to be read/written, and a state addressed so as to be the word lines except for the word line of the memory cells to be read and except for the word lines adjacent to the word line of the memory cells to be read.

Also, since in Article A, as described in the component 2c, "in the reading of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be read, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.9 V, the measurement voltage of the word line 24 is 6.4 V, the measurement voltage of the word line 25 is 0.48 V, the measurement voltage of the word line 26 is 6.4 V, and the measurement voltage of the word line 27 is 5.9 V" and "in the write verification of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be written, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.7 V, the measurement voltage of the word line 24 is 6.2 V, the measurement voltage of the word line 25 is 2.0 V, the measurement voltage of the word line 26 is 6.2 V, and the measurement voltage of the word line 27 is 5.7 V," it is reasonable to understand that it can be confirmed that also about the word lines except for the word lines 1, 20, and 26; namely, the word lines 0, 2 to 19, 21 to 25, and 27 to 31, similarly to the word lines 1, 20, and 26, when the values of addresses of memory cells to be read/written are incremented one by one, if measuring voltage, in the case that the word line is addressed so as to be a word line of the memory cells to be read/written, the measurement voltage is 0.48 V/2.0 V, in the case that the word line is addressed so as to be a word line adjacent to the word lines of the memory cells to be read/written, the measurement voltage is 6.4 V/6.2 V, and in the case that the word line is addressed to be a word line except for the word lines of the memory cells to be read/written and the word line adjacent to the word lines of the memory cells to be read, the measurement voltage is 5.9 V/5.7 V. Such understanding is supported from the measurement result shown in Evidence A No. 10 (a needle contact waveform measurement result report).

c According to the examination of b above, in Article A, in the case that the memory

cell of the word line 25 is addressed so as to be read/written, the word lines 0 to 22 and 28 to 31 correspond to the word lines when it is addressed so as to be a word line except for the word lines of the memory cells to be read/written and the word line adjacent to the word lines of the memory cells to be read, similarly to the word lines 23 and 27, so that it can be understood that if measuring voltage, it becomes 5.9 V/5.7 V.

Then, since in Article A, as described in the component 2c, "in the reading of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be read, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.9 V, the measurement voltage of the word line 24 is 6.4 V, the measurement voltage of the word line 25 is 0.48 V, the measurement voltage of the word line 26 is 6.4 V, and the measurement voltage of the word line 27 is 5.9 V" and "in the write verification of the NAND flash-memory, when a memory cell of a word line 25 of five continuous word lines 23 to 27 is addressed so as to be written, if measuring voltage about each word line of the word line 23, the word line 24, the word line 25, the word line 26, and the word line 27, the measurement voltage of the word line 23 is 5.7 V, the measurement voltage of the word line 24 is 6.2 V, the measurement voltage of the word line 25 is 2.0 V, the measurement voltage of the word line 26 is 6.2 V, and the measurement voltage of the word line 27 is 5.7 V," it can be understood that in Article A, "the first read pass voltage" lower than "the second read pass voltage" in "the two adjacent non-selected word lines adjacent to the selected word line" (the word lines 24 and 26) is applied to all "non-selected word lines except for the two adjacent non-selected word lines adjacent to the selected word line" (the word lines 0 to 23 and 27 to 31) among the non-selected word lines connected to the memory cells configuring one NAND string when the memory cell of the word line 25 is addressed so as to be read/written.

Then, it is reasonable that in Article A, it can be specified that "the second read pass voltage" of "the two adjacent non-selected word lines" "is higher" than "the first read pass voltage" of "the non-selected word lines except for the two adjacent non-selected word lines adjacent to the selected word line."

d Although the demandee alleges that the demandant merely shows the measurement results of CG 23 and CG 27 for "non-selected word lines which are not adjacent, non-selected word lines," and indicates no evidence about other "non-selected word lines," as described in b above, it can be understood that the same voltage as applied to word lines 23 and 27 is applied also to the word lines 0 to 22 and 28 to 31 which respectively correspond to the CG lines 0 to 22 and 28 to 31, so that it can be said that the demandant's proof is sufficient, and thus the allegation of the demandee discussed above cannot be accepted.

(B) Regarding the allegation of A (B) above

a According to a block diagram in a data sheet of "MX30UFxG26(28)AB" shown in Page 15 of Evidence A No. 3, it is reasonable to recognize that voltage is applied from a common high voltage circuit to any word line of Article A. Also, looking at the time course of the needle contact waveform of voltage on the five continuous word lines (the word lines 23 to 27), shown in a figure at the bottom of Page 13 of Evidence A No. 2, voltage change in the word line 25 corresponding to the selected word line and voltage

change in the word lines 24 and 26 corresponding to the adjacent non-selected word lines are different in the timing of turning from increase to decrease after measurement start, and according to this, it cannot be recognized that any interaction works between the voltage change in the word line 25 corresponding to the selected word line and the voltage change in the word lines 24 and 26 corresponding to the adjacent non-selected word lines. Then, in Article A, as slightly high voltage measured from the word lines 24 and 26 corresponding to the adjacent non-selected word lines was not caused by the voltage change in the word line 25 corresponding to the selected word line and other factors are not assumed in the investigation method related to Evidence A No. 2, it can be recognized that it is reasonable to understand that it was due to voltage application from the high voltage circuit.

Also, it is obvious that the measurement voltage of the word lines 23 and 27 corresponding to the non-selected word lines except for the adjacent non-selected word lines and the voltage measured from "the word lines 0 to 22 and 28 to 31" in "a NAND string having 32 floating gate nonvolatile memory cells connected in series" configuring "the NAND flash-memory," in Article A, are due to the voltage application from the high voltage circuit.

Then, it is reasonable that it can be specified that "the first read pass voltage" is applied from "the application" from "the drive circuit" and "the second read pass voltage which is higher than the first read pass voltage" is applied by "the application" from "the drive circuit" in Article A.

b Although the demandee alleges that it is obvious that it cannot be said that a factor causing a voltage rise (a difference between second voltage and first voltage) at the adjacent non-selected word lines of the selected word line can be other than the voltage application by the high voltage circuit, based on the fact that it is recognized that first read pass voltage is applied to the non-selected word lines except for two adjacent non-selected word lines adjacent to the selected word line, and second read pass voltage which is higher than the first read pass voltage is applied to the two adjacent non-selected word lines, without depending on the voltage application from the drive circuit, during the reading action of the NAND nonvolatile semiconductor memory described in Japanese Unexamined Patent Application Publication No. 2005-285185 (Evidence B No. 3) which is Cited Document 1 cited in the notice of reasons for refusal in the stage of examination on the patent, referring to the allegation in the written opinion (Evidence B No. 4) submitted by TOSHIBA CORPORATION as the applicant on March 15, 2010 in the stage of examination of the patent invention, in the reading action described in Evidence B No. 3, a voltage rise in the selected word line WLi and a voltage rise in the adjacent non-selected word lines WLi-1 and WLi+1 are synchronized at the rising timing, and are different from the time course of the needle contact waveform of voltage on the five continuous word lines (the word lines 23 to 27) shown in a figure below on Page 13 of Evidence No. 2, in a relationship between the timing of the voltage change in the selected word line and the timing of the voltage change in the adjacent non-selected word lines. Therefore, the description of Evidence B No. 3 cannot be a ground for proving that the measurement voltage change (the voltage rise on the word lines 24 and 26 corresponding to the adjacent non-selected word lines) on the five continuous word lines (the word lines 23 to 27) in Article A is caused by the same factors as that of the phenomena mentioned in Paragraphs [0075] and [0078] of

Evidence B No. 3. Then, since it is understood that the explanation in Evidence B No. 4 (the written opinion) excludes only the factors described in Evidence B No. 3 as being different from the factor of the voltage rise due to the voltage application from the drive circuit in the Patent, the allegation of the demandee based on the explanation in Evidence B No. 4 discussed above cannot be accepted.

(3) Accordingly, the component 2c of Article A satisfies the constituent component 2C of the patent invention.

4. Therefore, Article A satisfies the constituent component of Claim 2 according to the scope of claims for patent of the patent invention.

Also, none of the documentary evidences submitted by the demandant after the written refutation dated March 15, 2018 correspond to the replacement or alternation of the major facts, or the replacement or addition of direct evidences, and as described above, and none of them directly support the judgment, and thus it is obvious that it does not correspond to change in the gist of statement of the demand.

No. 5 Closing

As described above, Article A satisfies the constituent components 2A to 2D of Claim 2 according to the scope of claims for patent of the patent invention, so that Article A falls within the technical scope of the invention described in Claim 2 according to the scope of claims for patent of the patent invention.

Therefore, the advisory opinion shall be made as described in the conclusion.

デバイス情報

Table 1 Device Summary

Category	NAND Flash Memory
Manufacturer	Macronix
Fab.	Macronix own Fab. Fab5
Part Number	MX30UF4G28AB
Package Marking	MXIC S142606 MX30UF4G28AB-TI 8B223000B1
Package Type	TSOP 48
Package Size	18.4mm × 12.0mm = 220.8mm²
Die Marking	MXIC 2013 G3H6
Die Size	8.71mm × 6.88mm = 59.92mm²
Process Type	CMOS
Layers	2Poly—3Metal
Process Generation	36nm

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[Appendix: Page 4 of Evidence A No. 2]
デバイス情報 Device Information

[Appendix: Page 5 of Evidence A No. 2]

ＴＳＯＰ開口　TSOP Opening

報告書ＮＯ．Ｊ１ＦＡＡ１１３１４　Report No. J1FAA11314

開口と同時にＰＩが剥離される　PI is peeled at the time of opening

Figure 1 部分開封後の観察結果　Figure 1 Observation after partial opening

[Appendix: Page 6 of Evidence A No. 2]

ＦＩＢ加工箇所	FIB machining point
更新	updated

ＰＩ剥離（ＴＳＯＰ開口時）のみでＦＩＢ加工装置にて最上層配線が見える
Uppermost wiring layer is visible only by peeling PI (at the time of TSOP opening) with FIB machining device

[Appendix: Page 11 of Evidence A No. 2]
Needle Contact Waveform (Reading Action)

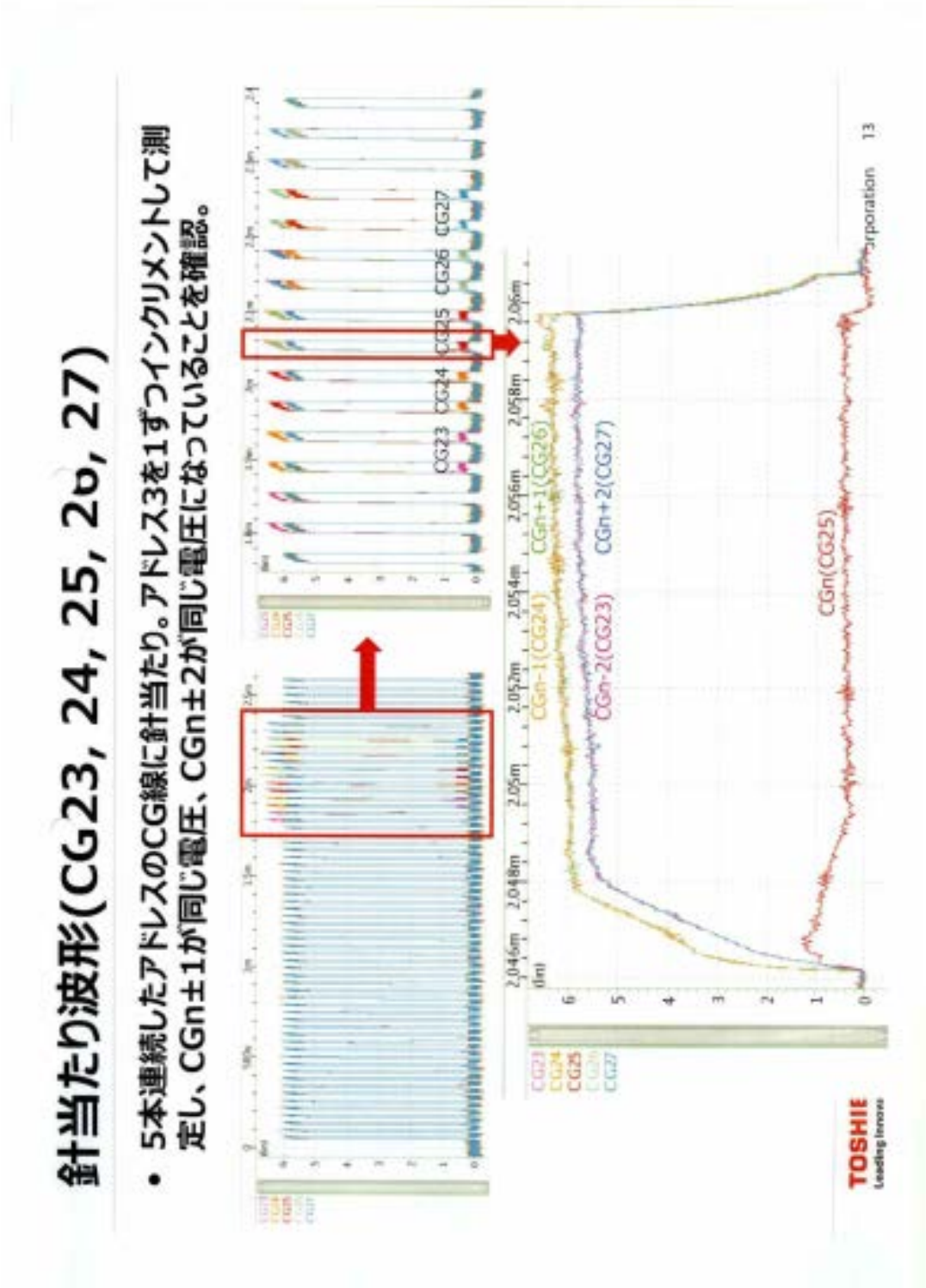
・VREADK is measured while address 3 is incremented one by one
・Selected twice for even and odd numbers
・VREAD=5.9V, VREADK=6.4V
・SGD, SGS: the same potential

[Appendix: Page 12 of Evidence A No. 2]
Needle Contact Waveform (Reading Action, Overlapped)

・There exist three types: first pass voltage (VREAD=5.9V), second pass voltage (VREADK=6.4V), and third pass voltage (SGD=SGS=4.1V).

・SGS is applied after first and second pass voltages, since SGS is recharged after discharge.

・CELSRC=VSS



[Appendix: Page 13 of Evidence A No. 2]
Needle Contact Waveform (CG23, 24, 25, 26, 27)
・A needle contact analysis of five CG lines with continuous addresses is carried out. Measured while address is incremented one by one, it is confirmed that CDn±1 have same voltage, and CDn±2 have same voltage.

[Appendix: Page 16 of Evidence A No. 2]
Needle Contact Waveform (Writing Action)

・Measured while address 3 is incremented one by one

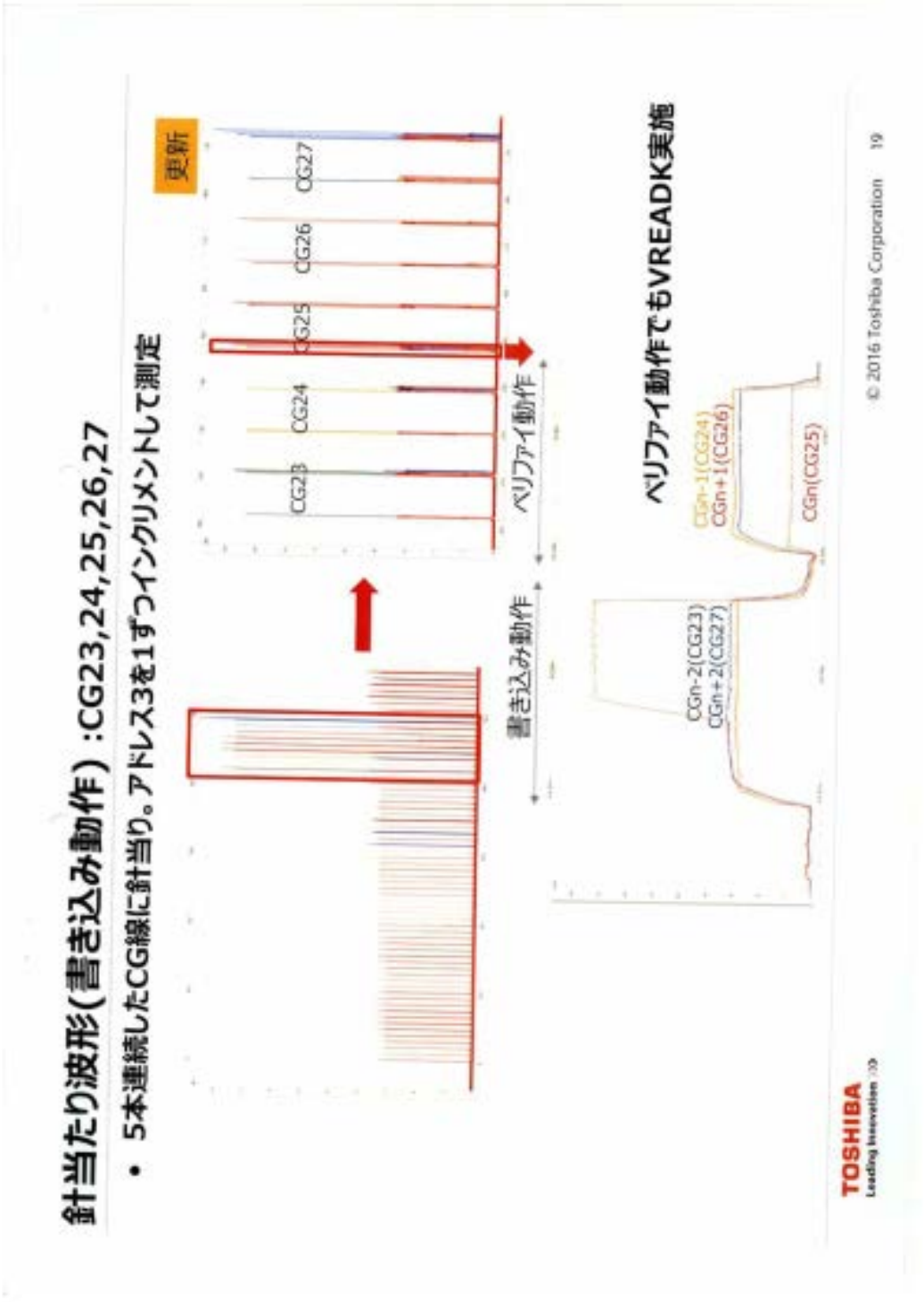
・Adjacent non-selected memory is written at the next timing.

[Appendix: Page 17 of Evidence A No. 2]
Needle Contact Waveform (Writing Action, Overlapped)

・VreadK is applied also at verify action.

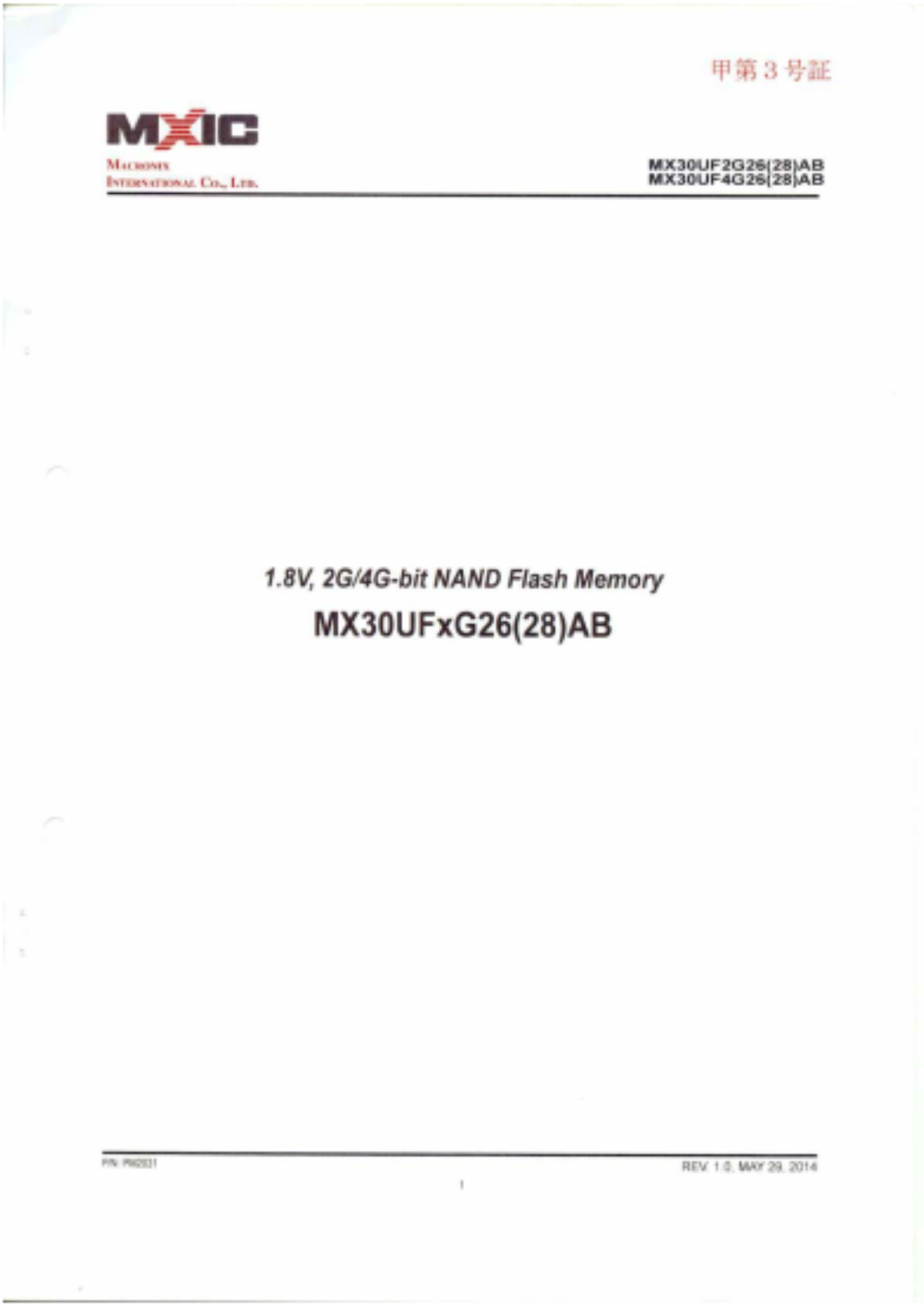
・Two adjacent non-selected WL (CDn±1) have same level.

[Appendix: Page 18 of Evidence A No. 2]
Needle Contact Waveform (Verifying Action, Magnified)
・Waveform is smoothed by 1 μ s to reduce noise.

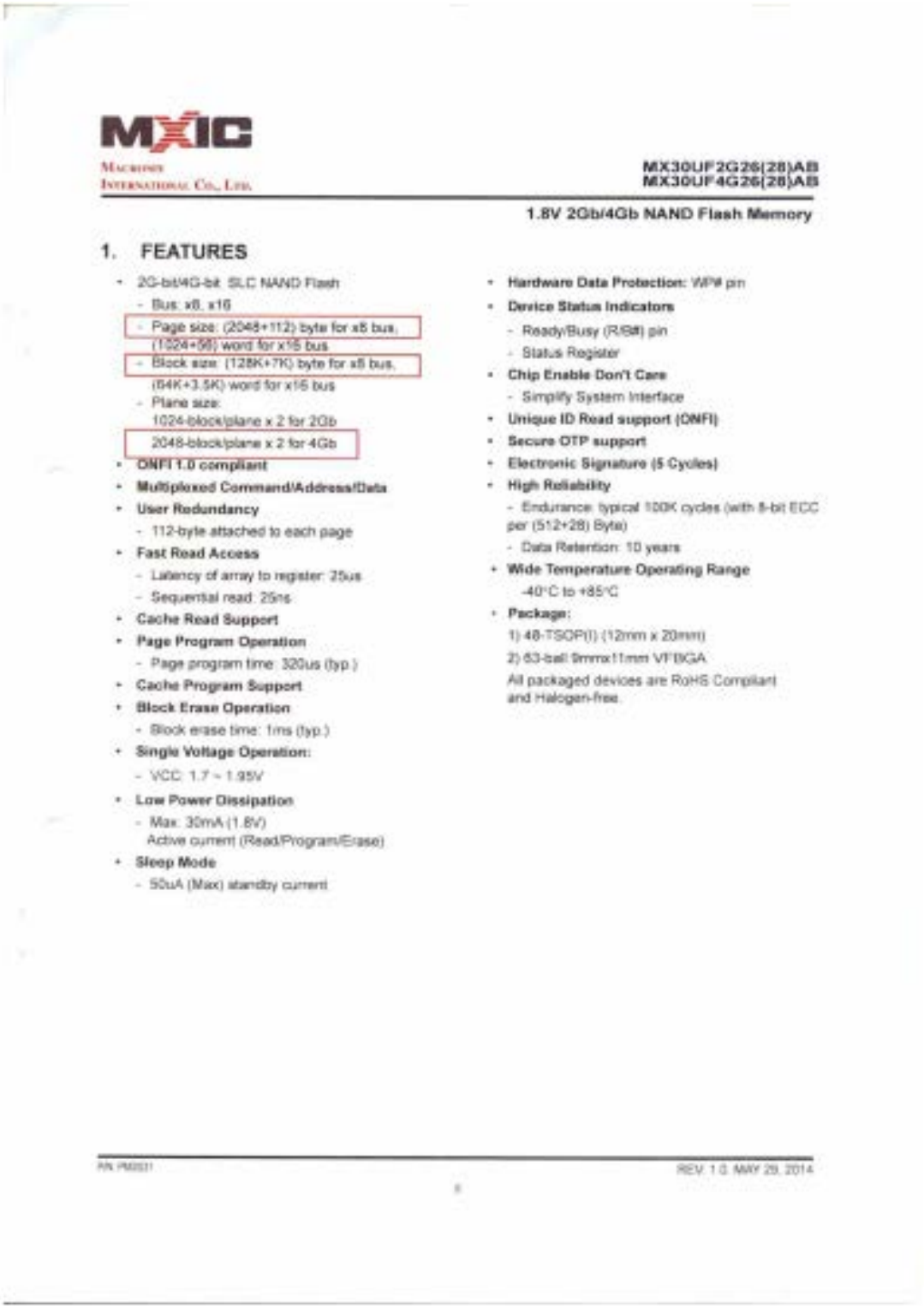


[Appendix: Page 19 of Evidence A No. 2]
Needle Contact Waveform (Writing Action) : CG23, 24, 25, 26, 27
・A needle contact analysis of five continuous CG lines is carried out. Measured while address is incremented one by one.

書き込み動作	writing action
ベリファイ動作	verifying action
ベリファイ動作でもＶＲＥＡＤＫ実施	VreadK is applied also at verify action



[Appendix: Page 1 of Evidence A No. 3]



MXIC
Macronix International Co., Ltd.

MX30UF2G26(28)AB
MX30UF4G26(28)AB

1.8V 2Gb/4Gb NAND Flash Memory

1. FEATURES

- 2G-bit/4G-bit SLC NAND Flash
  - Bus: x8, x16
  - Page size: (2048+112) byte for x8 bus, (1024+56) word for x16 bus
  - Block size: (128K+7K) byte for x8 bus, (64K+3.5K) word for x16 bus
  - Plane size:
    1024-block/plane x 2 for 2Gb
    2048-block/plane x 2 for 4Gb
- **ONFI 1.0 compliant**
- **Multiplexed Command/Address/Data**
- **User Redundancy**
  - 112-byte attached to each page
- **Fast Read Access**
  - Latency of array to register: 25us
  - Sequential read: 25ns
- **Cache Read Support**
- **Page Program Operation**
  - Page program time: 320us (typ.)
- **Cache Program Support**
- **Block Erase Operation**
  - Block erase time: 1ms (typ.)
- **Single Voltage Operation:**
  - VCC: 1.7 ~ 1.95V
- **Low Power Dissipation**
  - Max. 30mA (1.8V)
    Active current (Read/Program/Erase)
- **Sleep Mode**
  - 50uA (Max) standby current
- **Hardware Data Protection:** WP# pin
- **Device Status Indicators**
  - Ready/Busy (R/B#) pin
  - Status Register
- **Chip Enable Don't Care**
  - Simplify System Interface
- **Unique ID Read support (ONFI)**
- **Secure OTP support**
- **Electronic Signature (5 Cycles)**
- **High Reliability**
  - Endurance: typical 100K cycles (with 8-bit ECC per (512+28) Byte)
  - Data Retention: 10 years
- **Wide Temperature Operating Range**
  -40°C to +85°C
- **Package:**
  1) 48-TSOP(I) (12mm x 20mm)
  2) 63-ball 9mmx11mm VFBGA
  All packaged devices are RoHS Compliant and Halogen-free.

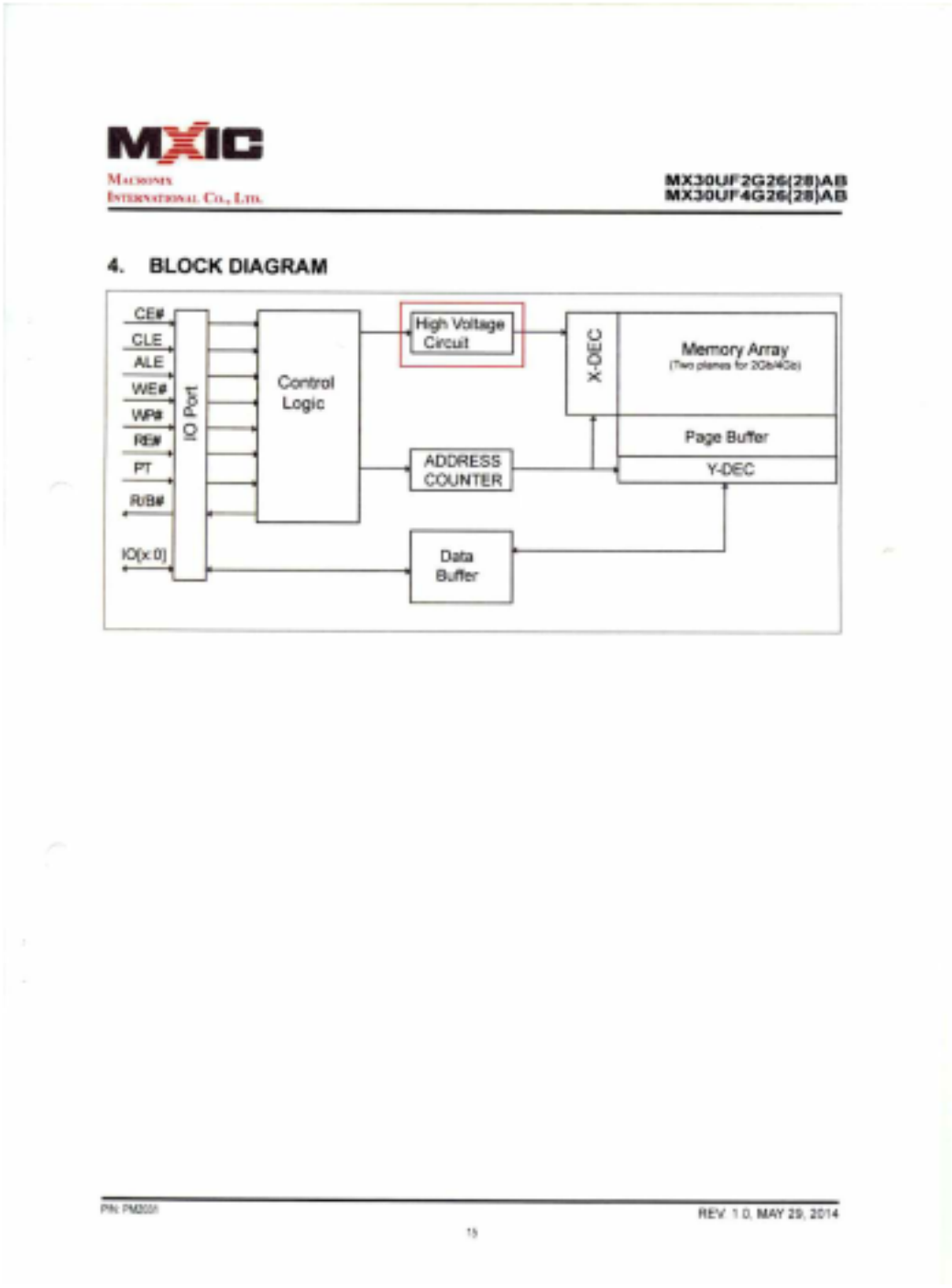
P/N: PM0931 REV. 1.0, MAY 29, 2014

[Appendix: Page 6 of Evidence A No. 3]

2-1. ORDERING INFORMATION

Part Name Description

[Appendix: Page 8 of Evidence A No. 3]



MXIC
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MX30UF2G26(28)AB
MX30UF4G26(28)AB

4. BLOCK DIAGRAM

P/N: PM2001
REV. 1.0, MAY 29, 2014
15

[Appendix: Page 15 of Evidence A No. 3]

July 27, 2018

Chief administrative judge: TSUJIMOTO, Yasutaka
Administrative judge: NAKAMA, Akira
Administrative judge: SUDA, Katsumi