Appeal decision

Appeal No. 2018-4523

Appellant Analog Devices, Inc.

Patent Attorney MURAYAMA, Yasuhiko

Patent Attorney JITSUHIRO, Shinya

Patent Attorney ABE, Tatsuhiko

The case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2014-6579, entitled "Differential Charge Reduction" (the application published on August 28, 2014, Japanese Unexamined Patent Application Publication No. 2014-158261) has resulted in the following appeal decision:

Conclusion

The appeal of the case was groundless.

Reason

No. 1 History of the procedures

The application was filed on January 17, 2014 (priority claim under the Paris Convention: February 15, 2013, (US)) and the history of the procedures is as follows.

February 10, 2016: Submission of written amendment

Dated September 1, 2016: Notice of reasons for refusal

October 11, 2016: Submission of written opinion

Dated March 31, 2017: Notice of reasons for refusal

June 26, 2017: Submission of written opinion and written amendment

Dated November 29, 2017: The examiner's decision of refusal

April 4, 2018: Appeal against the examiner's decision of refusal, submission of written amendment

Dated April 5, 2019: Notice of reasons for refusal by the body

July 4, 2019: Submission of written opinion and written amendment

No. 2 The Invention

The inventions according to claims of the present application are acknowledged as specified by the matters described in Claims 1 to 8 according to the scope of claims amended by the written amendment submitted on July 4, 2019, and the invention according to Claim 1 is as follows (hereinafter referred to as "the Invention").

"[Claim 1]

A device comprising:

an interleaved analog-to-digital converter stage, the interleaved analog-to-digital converter stage comprising:

an amplifier equipped with a non-inverted input and an inverted input; and

a plurality of channels, each of the plurality of channels including:

a pair of amplifier input switches, the pair of amplifier input switches including a first switch configured to receive a first switch input, to provide the first switch input to the non-inverted input of the amplifier when the switch is turned on, and to electrically insulate the non-inverted input of the amplifier from the first switch input when the switch is turned off, and a second switch configured to receive a second switch input, to provide the second switch input to the inverted input of the amplifier when the switch is turned on, and to electrically insulate the inverted input of the amplifier from the second switch when the switch is turned off; and

a pair of dummy circuit elements that is cross-linked between the input of the pair of amplifier input switches and the input of the amplifier, each dummy circuit element of the pair of dummy circuit elements having substantially the same capacitance as the first switch when the first switch is turned off,

wherein the pair of amplifier input switches on one of the plurality of channels is configured to provide charge to the non-inverted input and the inverted input of the amplifier, when the pair of amplifier input switches on the other of the plurality of channels is turned off, and

wherein the dummy circuit elements include capacitors."

No. 3 Reasons for refusal

Reason 3 of reasons for refusal notified by the body dated April 5, 2019 (hereinafter, referred to as "the reasons for refusal by the body") is that since the inventions according to Claims 1 to 13 of the present application could have been easily made before the application by a person who had ordinary skill in the art belonging to the Invention, on the basis of the invention described in following Cited Document 1

and the arts described in Cited Document 2 distributed in Japan or abroad before filing of the application or available to the public over an electric communication network, the Appellant should not be granted a patent under the provisions of Article 29(2) of the Patent Act.

Cited Document 1: U. S. Patent Application Publication No. 2012/0274497
Cited Document 2: Japanese Unexamined Patent Application Publication No. 2011-48885

No. 4 Cited Documents
1 Description in Cited Document 1 and Cited Invention

The specification of U. S. Patent Application Publication No. 2012/0274497 (hereinafter, referred to as "Cited Document 1") notified in the reasons for refusal by the body describes the following matters (Underlines were added by the body.).

(1) "[0001] The present invention is generally directed to pipelined analog-to-digital converters (ADCs). In particular, the present invention is directed to an ADC that includes a single amplifier selectively coupled to one of a plurality of copies of a circuit block in which each copy includes capacitors in different state of charge.

[0002] FIG. 1 illustrates an exemplary N-stage pipelined ADC 100 that is known in the art. The pipelined ADC 100 may include a number of cascaded multiplying digital-to-analog converter (MDAC) stages 102-108 and a control and correction logic circuit 110. The pipeline ADC 100 may receive an analog input signal vin at an input of the first stage 102 and eventually produce a digital output Dout that corresponds to vin. In operation, each stage of the pipelined ADC may be responsible for converting a portion of the input signal vin into a digital code and pass along a remaining portion of the input signal to a next stage of conversion. For example, stage i 106 may receive an input signal Vi-1 and convert the input signal into an n-bit digital code Di and output a remaining portion Vi of the input Vi-1 to the next stage i+1. The n-bit digital code Di may be a one-bit digital code, or a digital code of more than one bit. The control and correction logic 110 may receive the digital codes D1, D2, . . . , Di, . . . , Dn sequentially through a series of clock cycles (not shown) and assemble these digital codes into the digital output Dont. The assembling may include inserting appropriate delays and bit shifts. Further, the control and correction login 110 may correct digital errors."

(2) "[0024] FIG. 6 illustrates an MDAC stage 600 of a pipelined ADC according to an

exemplary embodiment of the present invention. The MDAC may include an amplifier 602 and four channels (channel 1-4) 604, 606, 608, 610. Each channel may be a copy of the same circuit block operating at a specific mode. Each channel may respectively include a flash (604.10, 606.10, 608.10, 610.10), an input capacitor (604.20, 606.20, 608.20, 610.20), a DAC capacitor (604.30, 606.30, 608.30, 610.30), and a feedback capacitor (604.40, 606.40, 608.40, 610.40). Four set of switches 612, 614, 616, 618 may be selectively engaged to couple the channels to input signal Vk-1 or to the amplifier 602. When a channel is coupled to the amplifier 602, the coupled channel and amplifier 602 may form a particular MDAC such as the one illustrated in FIG. 3.

[0025] During operation, in each clock cycle, the four channels 604, 606, 608, 610 may operate interleavingly in one of a sampling mode, a pre-gain mode, a gain mode, and a reset mode of the circuit block. FIG. 8 illustrates the interleaving operation modes of the four channels with respect to an ADC clock. For example, as illustrated in FIG. 8, during the first clock cycle, channel 1 may operate in the sample mode, channel 2 may run in the pre-gain mode, channel 3 may run in the gain mode, and channel 4 may run in the reset mode. It should be noted that the reset mode may also be a state of un-used mode while capacitor reset is accomplished during other modes. The un-used mode may be inserted for the purpose of randomization. During the second clock cycle, channel 1 operates in the pre-gain mode, channel 2 operates in the gain mode, channel 3 operates in the sample mode, and channel 4 operates in the reset mode. As shown in FIG. 8, the four channels operate interleavingly so that each of the four channels operates in one of the respective modes during a clock cycle. Further, with respect to a particular channel, the particular channel may sequence through sample, pre-gain, and gain in sequence while a random number of reset modes may be inserted after the gain mode."

(3) "[0030] In one embodiment of the present invention, channel 604 may also operate during a reset mode. During the reset mode, channel 604 may be disengaged from the input signal Vk-1 and from the amplifier 602 so that the comparator in the flash 604.10 and the DAC capacitor 604.30 may be reset during the reset mode."

(4) "[0035] FIG. 9 illustrates an exemplary circuit of an MDAC stage according to an embodiment of the present invention. FIG. 9 illustrates a circuit block of one channel. However, circuit blocks of other channels are similar and may be coupled to the illustrated channel in parallel. A common differential amplifier 902 may be selectively

coupled to one of the channels. Within the illustrated channel 900, the circuit block may include a 3-bit flash ADC 904, capacitors 906.10, 906.20, 908.10, 908.20, 910.10, 910.20, and switches 912.10, 912.20, 914, 916, 918.10, 918.20, 920, 922.10 to 922.40, 924, and 926. Capacitors 906.10, 906.20 are input capacitors that receive input signals. Capacitors 908.10, 908.20 are DAC capacitors. Capacitors 910.10, 910.20 are feedback capacitors. These switches are controllable so that they may be selectively engaged to transition the circuit block into one of a sample mode, a pre-gain mode, a gain mode, and a reset mode.

[0036] During the sample mode, the switches 912.10, 912.20, 916 may be engaged so that the input capacitors 906.10, 906.20 may be charged with the input signal. Also during the sample mode, the switches 914, 920 may be engaged so that the DAC capacitors 908.10, 908.20 and feedback capacitors 910.10, 910.20 may be reset. During the sample mode, all other switches are disengaged. Thus, the channel is decoupled from the amplifier 902.

[0037] During the pre-gain mode, the switch sets 918.10, 918.20 may be engaged so that the DAC capacitors 908.10, 908.20 may be charged. Since the 3-bit flash has 8 outputs, each of the switch sets 918.10, 918.20 may include eight switches. Further, the switch 926 may be engaged so that the charge on the input capacitors 906.10, 906.20 and DAC capacitors may be distributed during the pre-gain mode. During the pre-gain mode, all other switches are disengaged. Thus, the channel is decoupled from the amplifier 902.

[0038] The switch 924 may be engaged briefly with a pulse to reset the amplifier 902 at the beginning of every gain mode of each channel. Subsequent to the quick reset of the amplifier 902, the switches 922.10 to 922.40 may be engaged so that the feedback capacitors 910.10, 910.20 may be coupled to the amplifier 902, and the charge that is stored in the input capacitors 906.10, 906.20 may be transferred to the feedback capacitors 910.10, 910.20. Since the charge has been pre-distributed between the DAC capacitors 908.10, 908.20 and the input capacitors 906.10, 906.20, the transition to gain settling during gain mode is more linear and faster. In an alternative embodiment of the present invention, a reset clamp switch (not shown) may be coupled to the output node of the amplifier 902. The coupling of the output reset clamp switch may be in sync with the timing of the switch 924 to achieve even more linear settling for the amplifier 902."

(5) FIG. 1

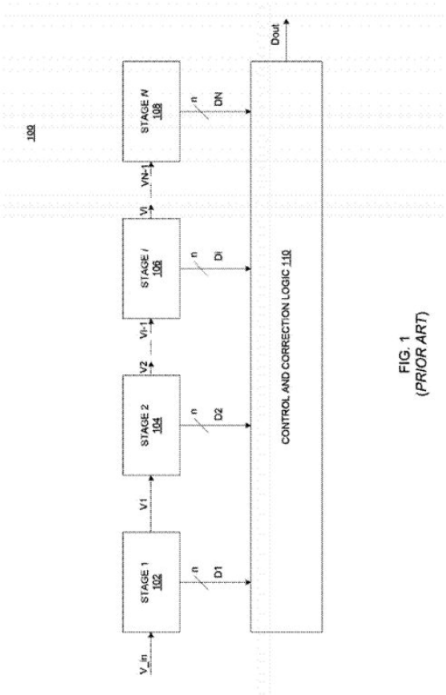


FIG. 1
(PRIOR ART)

(6) FIG. 6

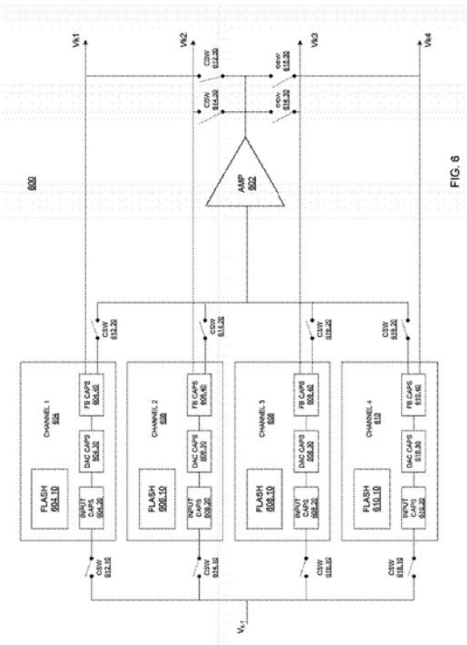


FIG. 8

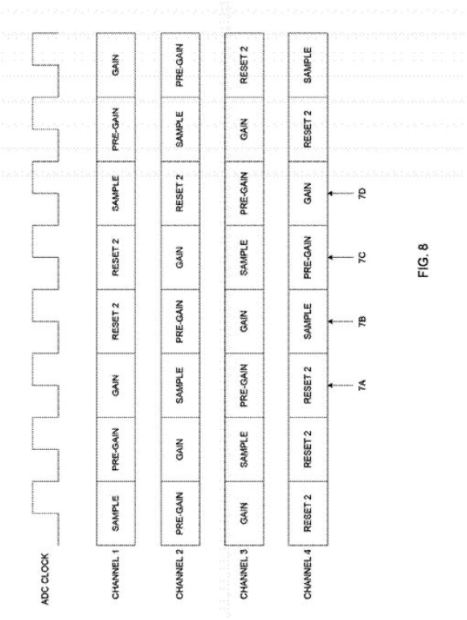


FIG. 8

(8) FIG. 9

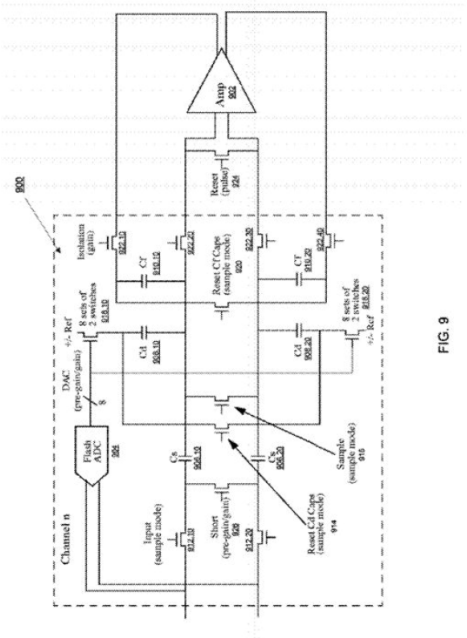


FIG. 9

In (4) [0035] above, it is described that a circuit shown in FIG. 9 illustrates a circuit block of one channel of a circuit of an MDAC stage, and similar circuit blocks of the other channel are connected in parallel. Further, it is described that the circuit block transits to each mode of sample, pre-gain, gain, and reset. Then, the circuit block of one channel of the MDAC stage described in (4), (8) above illustrates a

specific circuit configuration of one channel of the MDAC stage of the pipelined ADC described in (2) [0024] to [0025] above, and it can be said that in the plurality of channels, each circuit block performs interleaving operation. On the other hand, according to (1) above, the present invention is a "pipelined ADC", and the "pipelined ADC" is made by cascading MDAC stages.

Also, (8) FIG. 9 above shows that a differential amplifier 902 inputs two signals and outputs two signals.

Further, as described in (4) [0036] to [0038] above, the switches 922.10 to 922.40 are engaged in a gain mode, and according to (7) FIG. 8 above, only one of the channels in each ADC clock is in the gain mode, so that the switches 922.10 to 922.40 on one of the plurality of channels are engaged when the switches 922.10 to 922.40 on the other of the plurality of channels are disengaged.

Here, according to the description of (1) above, it can be said that "ADC" refers to "analog-to-digital converter," and "MDAC" is an abbreviation for "multiplying digital-to-analog converter".

Therefore, Cited Document 1 describes the following invention (hereinafter, referred to as "Cited Invention").

"A pipelined analog-to-digital converter, comprising:

a multiplying digital-to-analog converter stage with a 3-bit flash type analog-to-digital converter which operates in an interleave operation mode, the multiplying digital-to-analog converter stage comprising:

a differential amplifier 902 equipped with an input of two signals; and

a plurality of channels, each of the plurality of channels including:

two switches 922.20 and 922.30 including one switch 922.20 that is connected to one input of two inputs of the amplifier, can transfer charge collected in input capacitors 906.10 and 906.20 to feedback capacitors 910.10 and 910.20 in an engaged state, and separates the channel from the amplifier 902 in a disengaged state; and the other switch 922.30 that is connected to the other input of two inputs of the amplifier, can transfer charge collected in the input capacitors 906.10 and 906.20 in the engaged state, and separates the channel from the amplifier 902 in the disengaged state,

wherein the switches 922.20 and 922.30 on one channel of the plurality of channels are configured to be engaged when the switches 922.20 and 922.30 on the other channel of the plurality of channels are disengaged."

2 Description of Cited Document 2 and Art described in Cited Document 2

Japanese Unexamined Patent Application Publication No. 2011-48885 (hereinafter, referred to as "Cited Document 2") notified in the reasons for refusal by the body describes the following matters.

(1) "[0021]

Embodiment 1

Embodiment 1 of the present invention will be described with reference to the drawing. FIG. 1 is a block diagram showing a semiconductor memory device according to Embodiment 1 of the present invention. The circuit shown in FIG. 1 includes m×n (m and n are natural numbers) memory cells MC00 to MC(m−1)(n−1), n precharge circuits PC0 to PC(n−1), n column selectors CSR0 to CSR(n−1), n capacitance adding circuits DC0 to DC(n−1), one precharge circuit PCs, and one sense amplifier SA. Also, the circuit shown in FIG. 1 constitutes a memory cell array of mROW (row) and nCOLUMN (column). That is, n memory cells in the transverse direction (row direction) in FIG. 1, and m memory cells in the longitudinal direction (column direction) in FIG. 1 are arranged in a matrix to constitute a memory cell array.

[0022]

The memory cells are arranged at intersections between word lines WLs and bit line pairs DT/DBs. The m×n memory cells MC00 to MC(m−1)(n−1) are arranged in a matrix as a whole. Also, the word lines WLs are composed of word lines WL0 to WL(m−1). The bit line pairs DT/DBs are composed of bit line pairs DT0/DB0 to DT(n−1)/DB(n−1)."

(2) "[0026]

The bit line pair DT0/DB0 is connected to a READ line pair (common signal line pair) YDT/YDB through the precharge circuit PC0 and the column selector CSR0. Similarly, the bit line pair DT(n−1)/DB(n−1) is connected to the READ line pair YDT/YDB through the precharge circuit PC(n−1) and the column selector CSR(n−1). In this manner, the memory cell groups arranged in n columns are connected to the common READ line pair YDT/YDB through the corresponding precharge circuits PC0 to PC(n−1) and the corresponding column selectors CSR0 to CSR(n−1).

[0027]

The READ lines YDT/YDB are respectively connected to input terminals of the sense amplifier SA through the precharge circuit PCs for the sense amplifier. An output terminal of the sense amplifier SA is connected to an external output terminal of the semiconductor memory device. That is, the sense amplifier circuit SA amplifies a potential difference of the READ line pair YDT/YDB and outputs the amplified

potential difference as readout data from the memory cells.

[0028]

The column selector CSR0 includes a transistor (first switch element) T102 for selecting a column, and a transistor (second switch element) T103 for selecting a column. In this embodiment, an example where the transistors T102 and T103 are P-channel MOS transistors will be described."

(3) "[0033]

In the semiconductor memory device according to this embodiment, the parasitic capacitance added to YDT is set to be equal to the parasitic capacitance added to YDB. That is, the semiconductor memory device according to this embodiment is provided with the capacitance adding circuits so that the total parasitic capacitance between the bit line pairs DT/DBs and the READ line YDT becomes substantially equal to the total parasitic capacitance between the bit line pairs DT/DBs and the READ line YDB."

(4) "[0037]

That is, each transistor for selecting a column and the corresponding dummy transistor have substantially the same size. Thus, the parasitic capacitance existing between the source and the drain of each transistor for selecting a column which is in off state is substantially equal to the parasitic capacitance existing between the source and the drain of the corresponding dummy transistor. The source terminal of each transistor for selecting a column and the source terminal of the corresponding dummy transistor are connected to the respective READ lines (YDT, YDB). The drain terminal of each transistor for selecting a column and the drain terminal of the corresponding dummy transistor are each connected to the common bit line.

[0038]

For example, assume that the bit line pair DT1/DB1 is not selected. In this case, noise of the parasitic capacitance due to the effect of the transistor T106 is superimposed on YDT. Further, noise of the parasitic capacitance due to the effect of the transistor T105 is superimposed on YDB. Similarly, noise of the parasitic capacitance due to the effect of the transistor T107 is superimposed on YDB. Further, noise of the parasitic capacitance due to the effect of the transistor T108 is superimposed on YDT. The remaining non-selected columns (for example, DT2/DB2, DT3/DB3) have a similar relation."

(5) "[0057]

As is clear from the expression (6), the potential difference of the READ line pair YDT/YDB input to the sense amplifier SA in the case where the bit lines in the non-selected columns vary is the same as that in the case where no noise occurs (see FIG. 3D). That is, the READ line pair YDT/YDB offsets noise from the bit line pairs in the non-selected columns. Consequently, the semiconductor memory device according to this embodiment makes it possible to read out data accurately.

[0058]

Further, each transistor for selecting a column and each dummy transistor are P-channel MOS transistors. Thus, the semiconductor memory device enables provision of the same layout pattern for these transistors. That is, the parasitic capacitances of these transistors can be easily matched.

[0059]

As described above, when the parasitic capacitance added to the READ line YDT matches the parasitic capacitance added to the READ line YDB, the potential variation of the bit line DT1 induces noise equally in the READ lines YDT/YDB. At the same time, the potential variation of the bit line DB1 induces noise equally in the READ lines YDT/YDB. In short, the potential variation of each bit line induces noise equally in the READ lines YDT/YDB. Therefore, the noises are offset with each other. The same is true in the case of the other bit line pairs DT2/DB2 and DT3/DB3 in non-selected columns. In other words, regardless of the potential variation of the bit lines in non-selected columns, the potential difference between the READ lines YDT and YDB is equal to that in the case where no noise occurs. Therefore, the semiconductor memory device according to this embodiment can read out data accurately."

(6) "[0072]

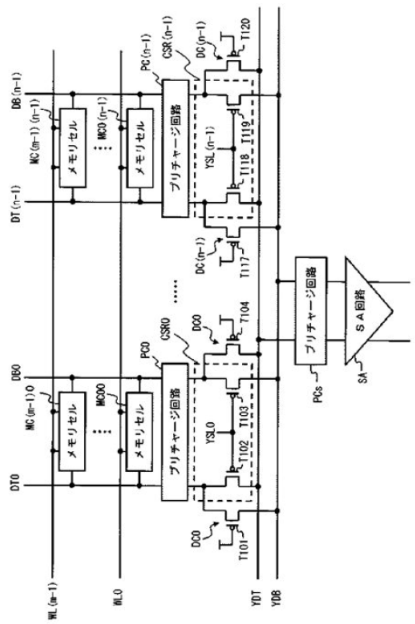
Note that the present invention is not limited to the above exemplary embodiments, but can be modified as appropriate within the scope of the present invention. For example, although the above-mentioned exemplary embodiments have described an example in which the column selectors and the capacitance adding circuits include dummy transistors or dummy transfer gates as dummy elements, the present invention is not limited thereto. The present invention is also applicable to a circuit configuration including capacitive elements (capacitors) which are substantially equal to the parasitic capacitance existing between the source and the drain when the corresponding transistors for selecting column (or the transfer gates for selecting column) are off, as dummy elements. FIG. 7 shows a specific example. The circuit shown in FIG. 7 includes capacitors C101, C104, C117, and C120 respectively in place

of the dummy transistors T101, T104, T117, and T120, as compared with the circuit shown in FIG. 1.

[0073]

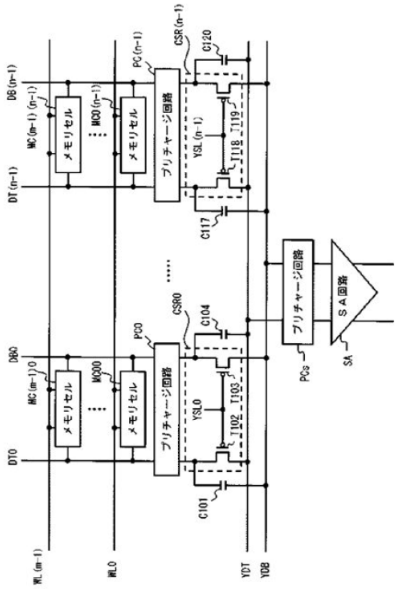
The capacitor C101 has one terminal connected to the bit line DT0, and the other terminal connected to the READ line YDB. The capacitor C104 has one terminal connected to the bit line DB0, and the other terminal connected to the READ line YDT. The capacitor C117 has one terminal connected to the bit line DT(n−1), and the other terminal connected to the READ line YDB. The capacitor C120 has one terminal connected to the bit line DB(n−1), and the other terminal connected to the READ line YDT. This circuit configuration also provides the same effects as those of the circuit shown in FIG. 1."

(7) FIG. 1



メモリセル	Memory Cell
プリチャージ回路	Precharge Circuit
ＳＡ回路	SA Circuit

(8) FIG. 7



メモリセル	Memory Cell
プリチャージ回路	Precharge Circuit
ＳＡ回路	SA Circuit

According to the description "the sense amplifier circuit SA amplifies a potential difference of the READ line pair YDT/YDB" in (2) [0027] above, the sense amplifier circuit is a differential amplifier.

According to (2) [0027], (6) [0072] to [0073], and (8) FIG. 7 above, the dummy elements C101 and C104 made from a pair of capacitors are cross-linked between the input side of the pair of switch elements T102 and T103 connected to the pair of inputs of the sense amplifier circuit and the pair of inputs of the sense amplifier circuit.

From the above, it is recognized that Cited Document 2 describes "the art which cross-links a pair of dummy elements between an input side of a pair of switch elements to be connected to a pair of inputs of differential amplifiers and the pair of inputs of differential amplifiers, makes a capacitor with capacitance substantially equal to a parasitic capacitance when the switch elements are in an off-state, as the dummy elements, thereby offsetting noise due to the parasitic capacitance when the switch elements are in the off-state" (hereinafter, referred to as "the well-known art").

No. 5 Comparison

The Invention and the Cited Invention are compared.

1 "A pipelined analog-to-digital converter" of Cited Invention is included in "a device"

of the Invention.

2 Since "a multiplying digital-to-analog converter stage" of Cited Invention performs analog-to-digital conversion processing by "a 3-bit flash type analog-to-digital converter" in the multiplying digital-to-analog converter stage, it can be optionally referred to as "an analog-to-digital converter stage" of the Invention.

3 The input of two signals of "a differential amplifier" is generally referred to as "an inverted input" and "a non-inverted input". Therefore, "a differential amplifier 902 equipped with an input of two signals" of Cited Invention corresponds to "an amplifier equipped with a non-inverted input and an inverted input."

4 Regarding "two switches 922.20 and 922.30" of Cited Invention, respective switches are connected to the input of the amplifier, so that they correspond to "a pair of amplifier input switches" of the Invention.

Since "in an engaged state" of the switch of Cited Invention, the switch "can transfer charge collected in input capacitors 906.10 and 906.20 to feedback capacitors 910.10 and 910.20," it is when the switch is turned on, and it can be said an state that the input of the switch is provided to one of the inputs of the two signal of the amplifier. Also, since "in a disengaged state" of the switch, the switch "separates the channel from the amplifier 902," it is when the switch is turned off, and it can be said an state that the input of the switch and one of the inputs of the two signals of the amplifier are electrically insulated.

Therefore, "one switch 922.20 that is connected to one input of two inputs of the amplifier, can transfer charge collected in input capacitors 906.10 and 906.20 to feedback capacitors 910.10 and 910.20 in an engaged state, and separates the channel from the amplifier 902 in a disengaged state" of Cited Invention corresponds to "a first switch configured to receive a first switch input, to provide the first switch input to the non-inverted input of the amplifier when the switch is turned on, and to electrically insulate the non-inverted input of the amplifier from the first switch input when the switch is turned off" of the Invention.

Similarly, "the other switch 922.30 that is connected to the other input of the two inputs of the amplifier, can transfer charge collected in the input capacitors 906.10 and 906.20 to feedback capacitors 910.10 and 910.20 in the engaged state, and separates the channel from the amplifier 902 in the disengaged state" of Cited Invention corresponds to "a second switch configured to receive a second switch input, to provide the second switch input to the inverted input of the amplifier when the switch is turned on, and to electrically insulate the inverted input of the amplifier from the second switch when the switch is turned off" of the Invention.

Then, the Invention and Cited Invention are common in the point of "a device comprising:

an interleaved analog-to-digital converter stage, the interleaved analog-to-digital converter stage comprising:

an amplifier equipped with a non-inverted input and an inverted input; and

a plurality of channels, each of the plurality of channels including:

a pair of amplifier input switches, the pair of amplifier input switches including a first switch configured to receive a first switch input, to provide the first switch input to the non-inverted input of the amplifier when the switch is turned on, and to electrically insulate the non-inverted input of the amplifier from the first switch input when the switch is turned off, and a second switch configured to receive a second switch input, to provide the second switch input to the inverted input of the amplifier when the switch is turned on, and to electrically insulate the inverted input of the amplifier from the second switch when the switch is turned off,

wherein the pair of amplifier input switches on one of the plurality of channels is configured to provide charge to the non-inverted input and the inverted input of the amplifier, when the pair of amplifier input switches on the other of the plurality of channels is turned off," and differ in the following point.

Different Feature:

In the Invention, each of the plurality of channels includes "a pair of dummy circuit elements that is cross-linked between the input of the pair of amplifier input switches and the input of the amplifier, each dummy circuit element of the pair of dummy circuit elements having substantially the same capacitance as the first switch when the first switch is turned off," and "the dummy circuit elements include capacitors," whereas, Cited Invention does not have this configuration.

No. 6 Judgment

The above-mentioned Different Feature is examined.

Since it is a common technical matter that noise is generated by leakage of a charge due to a parasitic capacitance in a switch in the off state, and the switches 922.20 and 922.30 in Cited Invention are switches that may be brought into the disengaged state, it is obvious that noise due to a parasitic capacitance is generated when the switches are in the off state, so that as a means for solving the obvious problem, a person skilled in the art could have easily made the Invention, by applying "the art which cross-links a pair of dummy elements between an input side of a pair of switch

elements to be connected to a pair of inputs of differential amplifiers and the pair of inputs of amplifiers, makes a capacitor with capacitance substantially equal to a parasitic capacitance when the switch elements are in an off-state, as the dummy elements, thereby offsetting noise due to the parasitic capacitance when the switch elements are in the off-state."

No.7 Appellant's allegation

The appellant, in the written opinion submitted on July 04, 2019, alleges that "in Cited Document 1, during a sample mode, a switch 916 is brought into an engaged state, so that the electric potentials on the amplifier 902 side of the input capacitors 906.10 and 906.20 become the same. During the pre-gain mode, the switch 926 is brought into the engaged state, so that the electric potentials on the input side of the input capacitors 906.10 and 906.20 become the same. At that time, the switch 916 is in a disengaged state, signs of the electric potentials on the amplifier 902 side of the input capacitors 906.10 and 906.20 are different, and the electric potentials come to have the same strength. Therefore, charges leaked through the switches 922.20 and 922.30 are offset with each other by resetting at the beginning of the gain mode. Consequently, there is no motivation to apply the technology disclosed in Cited Document 2 to the invention disclosed in Cited Document 1."

However, in the switch in the disengaged state, as the appellant also describes as "charges leaked through the switches 922.20 and 922.30", it is a common technical matter that a charge due to the parasitic capacitance leaks to generate noise, so that also in Cited Invention, during the pre-gain mode, it is obvious that similar noise is generated in the switches 922.20 and 922.30 in the disengaged state.

Therefore, there is a motivation to apply the technology disclosed in Cited Document 2 which offsets the noise by the leakage of a charge due to the parasitic capacitance.

Accordingly, the allegation of the appellant cannot be accepted.

No. 8 Closing

As described above, since the Invention could have been easily made before filing of the application by a person who had ordinary skill in the art belonging to the Invention, on the basis of the invention described in following Cited Document 1 and the arts described in Cited Document 2 distributed in Japan or abroad or available to the public over an electric communication network before filing of the application, the Appellant should not be granted a patent under the provisions of Article 29(2) of the

Patent Act.

Therefore, the appeal decision shall be made as described in the conclusion.

November 18, 2019

Chief administrative judge: YOSHIDA, Takayuki
Administrative judge: IBATO, Fumihiko
Administrative judge: OKAMOTO, Masaki