Appeal decision

Appeal No. 2018-13073

Appellant Samsung Display

Patent Attorney Kyosei International Patent Firm

The case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2017-1414, entitled "DISPLAY PANEL AND DISPLAY APPARATUS INCLUDING THE SAME" (the application published on April 13, 2017, Japanese Unexamined Patent Application Publication No. 2017-72858) has resulted in the following appeal decision.

Conclusion

The appeal of the case was groundless.

Reason

No. 1 History of the procedures

The application relating to the case of appeal (hereinafter referred to as "the Application") claims priority under the Paris Convention based on the patent application filed in South Korea on February 23, 2011 (hereinafter referred to as "Priority date"), and the Application is a divisional application filed on January 6, 2017 claiming the priority from a patent application (Japanese Patent Application No. 2012-30124) filed on February 15, 2012.

The Specification and the Scope of Claims were amended on February 2, 2017. Furthermore, the Specification and the Scope of Claims were amended on December 29, 2017 (hereinafter referred to as "First amendment"), and a written opinion (hereinafter referred to as "First written opinion") was submitted. An examiner's decision of refusal was issued on May 18, 2018. A certified copy of the examiner's decision was delivered on May 29, 2018.

Against this, an appeal against the examiner's decision of refusal (the appeal of the case) was requested on October 1, 2018, and the Specification and the Scope of Claims were amended at the same time. This amendment was dismissed by a decision dated June 20, 2019, and a notice of reasons for refusal (hereinafter referred to as "Reasons for

refusal by the body") was issued on the same day. This notice of reasons for refusal is the final notice of reasons for refusal stipulated in Article 17-2(1)(iii) of the Patent Act.

An amendment (hereinafter referred to as "the Amendment") on the Specification and the Scope of Claims was made on September 25, 2019, and a written opinion (hereinafter referred to as "the Written opinion") was submitted.

The number of claims before the Amendment (i.e., after the First amendment, the same applies hereinafter) is 10, and the number of claims after the Amendment is 2.

No. 2 Decision to dismiss amendment

[Conclusion of Decision to Dismiss Amendment]

The Amendment shall be dismissed.

[Reason for Decision to Dismiss Amendment]

As described below, the Amendment, which is not intended for the matters listed in any of the items of Article 17-2(5)(i) to (iv)of the Patent Act, shall be dismissed under the provisions of Article 53(1) of the Patent Act applied mutatis mutandis by replacing certain terms pursuant to Article 159(1) of the Patent Act.

1 Details of the Amendment

The Amendment includes: as a first amended matter, deleting Claims 1 to 7 and Claim 9 before the Amendment; and, as a second amended matter, deleting a part of the description in Claim 8 before the Amendment and adding the descriptions of Claim 3 and Claim 9 before the Amendment to the above description, as Claim 1 after the Amendment. The Amendment also includes, as a third amended matter, modifying Claim 10 before the Amendment described with reference to the description of Claim 8 to refer to the description of Claim 1 after the Amendment, as Claim 2 after the Amendment.

Therefore, Claim 1 and Claim 2 after the Amendment correspond to Claim 8 and Claim 10 before the Amendment, respectively.

The partial deletion of description of Claim 8 before the Amendment and the addition of description of Claim 3 before the Amendment in the second amended matter of the Amendment are amended matters on the "first discharging transistor", the "second discharging transistor", the "(i-1)-th stage", and the "j-th stage". The addition of description of Claim 9 before the Amendment is an amended matter on the "printed circuit board".

The descriptions of Claim 8 before the Amendment and Claim 1 after the Amendment are as follows. For convenience of reference, descriptions of Claim 3 and

Claim 9 before the Amendment are also presented. The underlines were added by the body for indicating amended matters on the "first discharging transistor" and the "second discharging transistor" in the second amended matter of the Amendment, or for indicating the part deleted from Claim 8 before the Amendment and the description of Claim 3 before the Amendment added to the description of Claim 8 before the Amendment.

(1) Before the Amendment

"[Claim 3]

The display panel of Claim 1, wherein the (i-1)-th stage and the second discharging transistor are formed in the first peripheral area so as to have a width smaller than or equal to a width of the first pixel row defined by first and second gate lines of the first pixel row, and

the j-th stage and the first discharging transistor are formed in the second peripheral area so as to have a width smaller than or equal to a width of the second pixel row defined by the first and second gate lines of the second pixel row."

"[Claim 8]

A display apparatus comprising:

a display panel including a plurality of pixels arranged in the display area and comprising a plurality of pixel rows having a first pixel row and a second pixel row and a plurality of pixel columns, a plurality of data lines including an (m-1)-th data line, an m-th data line, an (m+1)-th data line, and an (m+2)-th data line (m is a natural number) which extend in a column direction and are arranged sequentially, a plurality of gate lines which extend in a row direction, a first gate driving circuit formed in a first peripheral area of the display area, and a second gate driving circuit formed in a second peripheral area of the display area opposite to the first peripheral area; and

a printed circuit board which is electrically connected to the display panel, and has a main driving circuit which generates a first clock signal, a second clock signal, a third clock signal, and a fourth clock signal to be provided to the first and second gate driving circuits, wherein

the first pixel row is arranged between a first gate line located at a first side of the first pixel row and a second gate line located at a second side of the first pixel row,

the second pixel row is arranged between a first gate line adjacent to the first pixel row and located at a first side of the second pixel row and a second gate line located at a second side of the second pixel row,

the first gate driving circuit includes an (i-1)-th stage (i is a natural number) which

is formed in the first peripheral area of the display area and provides a gate signal to the first gate line of the first pixel row and an i-th stage which is adjacent to the (i-1)-th stage and provides a gate signal to the first gate line of the second pixel row,

the display panel comprises a second discharging transistor which is formed in the first peripheral area between the (i-1)-th stage and the i-th stage and discharges a high voltage applied to the second gate line of the first pixel row to a low voltage,

first and second pixels in the first pixel row between the (m-1)-th data line and the m-th data line are electrically connected to the m-th data line,

third and fourth pixels in the first pixel row between the m-th data line and the (m+1)-th data line are electrically connected to the (m+1)-th data line,

fifth and sixth pixels in the first pixel row between the (m+1)-th data line and the (m+2)-th data line are electrically connected to the (m+2)-th data line,

the first, third, and sixth pixels of the first pixel row are electrically connected to the first gate line located at the first side of the first pixel row,

the second, fourth, and fifth pixels of the first pixel row are electrically connected to the second gate line located at the second side of the first pixel row,

the second gate driving circuit includes a (j-1)-th stage (j is a natural number) which is formed in the second peripheral area and provides a gate signal to the second gate line of the first pixel row, and a j-th stage which is formed in the second peripheral area adjacent to the (j-1)-th stage and provides a gate signal to the second gate line of the second pixel row,

the display panel further comprises a first discharging transistor which is formed in the second peripheral area between the (j-1)-th stage and the j-th stage and discharges a high voltage applied to the first gate line of the second pixel row to a low voltage, and

the first discharging transistor does not overlap the second discharging transistor in the row direction.

[Claim 9]

The display apparatus of Claim 8, wherein

the printed circuit board comprises:

first signal lines which transmit the first and second clock signals to the first gate driving circuit;

second signal lines which transmit the third and fourth clock signals to the second gate driving circuit; and

an RC control part controlling a time constant of the first and second signal lines."

(2) After the Amendment

"[Claim 1]

A display apparatus comprising:

a display panel including a plurality of pixels arranged in the display area and comprising a plurality of pixel rows having a first pixel row and a second pixel row and a plurality of pixel columns, a plurality of data lines including an (m-1)-th data line, an m-th data line, an (m+1)-th data line, and an (m+2)-th data line (m is a natural number) which extend in a column direction and are arranged sequentially, a plurality of gate lines which extend in a row direction, a first gate driving circuit formed in a first peripheral area of the display area, and a second gate driving circuit formed in a second peripheral area of the display area opposite to the first peripheral area; and

a printed circuit board which is electrically connected to the display panel, and has a main driving circuit which generates a first clock signal, a second clock signal, a third clock signal, and a fourth clock signal to be provided to the first and second gate driving circuits, wherein

the first pixel row is arranged between a first gate line located at a first side of the first pixel row and a second gate line located at a second side of the first pixel row,

the second pixel row is arranged between a first gate line adjacent to the first pixel row and located at a first side of the second pixel row and a second gate line located at a second side of the second pixel row,

the first gate driving circuit includes an (i-1)-th stage (i is a natural number) which is formed in the first peripheral area of the display area and provides a gate signal to the first gate line of the first pixel row, and an i-th stage which is adjacent to the (i-1)-th stage and provides a gate signal to the first gate line of the second pixel row,

the display panel comprises a second discharging transistor which is formed in the first peripheral area between the (i-1)-th stage and the i-th stage and discharges a high voltage applied to the second gate line of the first pixel row to a low voltage,

first and second pixels in the first pixel row between the (m-1)-th data line and the m-th data line are electrically connected to the m-th data line,

third and fourth pixels in the first pixel row between the m-th data line and the (m+1)-th data line are electrically connected to the (m+1)-th data line,

fifth and sixth pixels in the first pixel row between the (m+1)-th data line and the (m+2)-th data line are electrically connected to the (m+2)-th data line.

the first, third, and sixth pixels of the first pixel row are electrically connected to the first gate line located at the first side of the first pixel row,

the second, fourth, and fifth pixels of the first pixel row are electrically connected to the second gate line located at the second side of the first pixel row,

the second gate driving circuit includes a (j-1)-th stage (j is a natural number) which is formed in the second peripheral area and provides a gate signal to the second gate line of the first pixel row, and a j-th stage which is formed in the second peripheral area adjacent to the (j-1)-th stage and provides a gate signal to the second gate line of the second pixel row,

the display panel further comprises a first discharging transistor which is formed in the second peripheral area between the (j-1)-th stage and the j-th stage and discharges a high voltage applied to the first gate line of the second pixel row to a low voltage,

the (i-1)-th stage and the second discharging transistor are formed in the first peripheral area so as to have a width smaller than or equal to a width of the first pixel row defined by first and second gate lines of the first pixel row,

the j-th stage and the first discharging transistor are formed in the second peripheral area so as to have a width smaller than or equal to a width of the second pixel row defined by the first and second gate lines of the second pixel row,

the printed circuit board comprises:

first signal lines which transmit the first and second clock signals to the first gate driving circuit;

second signal lines which transmit the third and fourth clock signals to the second gate driving circuit; and

an RC control part controlling a time constant of the first and second signal lines."

2 Purpose of Amendment

(1) Judgment

A The amended matters on the "first discharging transistor", the "second discharging transistor", the "(i-1)-th stage", and the "j-th stage" in the second amended matter of the Amendment are, specifically, deleting the description, "the first discharging transistor does not overlap the second discharging transistor in the row direction" (hereinafter referred to as "Description before amendment"), and adding the description, "the (i-1)-th stage and the second discharging transistor are formed in the first peripheral area so as to have a width smaller than or equal to a width of the first pixel row defined by first and second gate lines of the first pixel row" (hereinafter referred to as "Description after amendment 1"), and the description, "the j-th stage and the first discharging transistor are formed in the second peripheral area so as to have a width smaller than or equal to a width of the second pixel row defined by the first and second gate lines of the second pixel row" (hereinafter referred to as "Description after amendment 2").

B The Description before amendment specifies a positional relationship in the row direction between the "first discharging transistor" and the "second discharging transistor".

The Description after amendment 1 specifies a dimensional relationship between the width of the "(i-1)-th stage" and the "second discharging transistor" and the "width of the first pixel row" "defined by first and second gate lines of the first pixel row". Similarly, the Description after amendment 2 specifies a dimensional relationship between the width of the "j-th stage" and the "first discharging transistor" and the "width of the second pixel row" "defined by the first and second gate lines of the second pixel row".

Therefore, the amended matters on the "first discharging transistor", the "second discharging transistor", the "(i-1)-th stage", and the "j-th stage" are deleting specification of positional relationship in the row direction between the "first discharging transistor" and the "second discharging transistor", and adding specification of dimensional relationship between the width of the "(i-1)-th stage" and the "second discharging transistor" and the "width of the first pixel row" "defined by first and second gate lines of the first pixel row", and the width of the "j-th stage" and the "first discharging transistor" and the "width of the second pixel row" "defined by the first and second gate lines of the second pixel row".

However, there is a significant difference in point of view between the specification of positional relationship and the specification of dimensional relationship, and it cannot be acknowledged that the specification of positional relationship in the Description before amendment is substantially maintained even after the Amendment by the specification of dimensional relationship in the Description after amendment 1 and the Description after amendment 2. Thus, even if the dimensional relationship between the width of the "(i-1)-th stage" and the "second discharging transistor" and the "width of the first pixel row" "defined by first and second gate lines of the first pixel row" and the width of the "j-th stage" and the "first discharging transistor" and the "width of the second pixel row" "defined by the first and second gate lines of the second pixel row" are specified in place of the positional relationship in the row direction between "the first discharging transistor" and the "second discharging transistor", the positional relationship in the row direction between the "first discharging transistor" and the "second discharging transistor" is not limited as compared with before the Amendment. Ambiguity of positional relationship in the row direction between the "first discharging transistor" and the "second discharging transistor" is also not eliminated.

C Accordingly, it is obvious that the amended matters on the "first discharging transistor", the "second discharging transistor", the "(i-1)-th stage", and the "j-th stage" in the second amended matter of the Amendment do not fall under the restriction of the scope of claims, clarification of an ambiguous statement, deletion of a claim or claims, or correction of errors.

(2) Appellant's allegation

The appellant alleges in the written opinion that the Amendment is to conform the claims to the description of the specification, aiming for restriction of components in a limited way and clarification of an ambiguous statement by integration of claims.

However, it cannot be said that the Amendment, which deletes a part of the description of Claim 8 before the Amendment (Description before amendment) as well as adding the description of Claim 3 before the Amendment (Description after amendment 1 and Description after amendment 2) and the description of Claim 9 before the Amendment to the description of Claim 8 before the Amendment, is integration of claims, immediately. The amendment to delete the Description before amendment and add the Description after amendment 1 and Description after amendment 2 does not fall under the restriction of the scope of claims or clarification of an ambiguous statement, as described in (1).

Therefore, the appellant's allegation cannot be accepted.

3 Closing on the decision to dismiss amendment

As described above, the Amendment is not intended for the matters listed in any of the items of Article 17-2(5)(i) to (iv)of the Patent Act.

Therefore, the Amendment shall be dismissed under the provisions of Article 53(1) of the Patent Act applied mutatis mutandis by replacing certain terms pursuant to Article 159(1) of the Patent Act.

Thus, the decision is made in accordance to Conclusion of Decision to Dismiss Amendment.

No. 3 Judgment on the Application

1 Description of the Scope of Claims

As described in No. 2, the Amendment was dismissed. The description of the Scope of Claims of the Application is as described in the Scope of Claims after the First amendment. Especially, the description of Claim 1 after the First amendment is as follows.

Hereinafter, the invention specified by the matters described in Claim after the First amendment is referred to as "the Invention".

"[Claim 1]
A display panel comprising:

a plurality of pixels arranged in a display area and comprising a first pixel row and a second pixel row;

a plurality of data lines including an (m-1)-th data line, an m-th data line, an (m+1)-th data line, and an (m+2)-th data line (m is a natural number) which extend in a column direction and are arranged sequentially; and

a plurality of gate lines which extend in a row direction, wherein

the first pixel row is arranged between a first gate line located at a first side of the first pixel row and a second gate line located at a second side of the first pixel row,

the second pixel row is arranged between a first gate line located at a first side of the second pixel row and a second gate line located at a second side of the second pixel row,

an (i-1)-th stage (i is a natural number) which is formed in a first peripheral area of the display area and provides a gate signal to the first gate line of the first pixel row,

an i-th stage which is formed in the first peripheral area adjacent to the (i-1)-th stage and provides a gate signal to the first gate line of the second pixel row, and

a second discharging transistor which is formed in the first peripheral area between the (i-1)-th stage and the i-th stage and discharges a high voltage applied to the second gate line of the first pixel row to a low voltage, wherein

first and second pixels in the first pixel row between the (m-1)-th data line and the m-th data line are electrically connected to the m-th data line,

third and fourth pixels in the first pixel row between the m-th data line and the (m+1)-th data line are electrically connected to the (m+1)-th data line,

fifth and sixth pixels in the first pixel row between the (m+1)-th data line and the (m+2)-th data line are electrically connected to the (m+2)-th data line,

the first, third, and sixth pixels of the first pixel row are electrically connected to the first gate line located at the first side of the first pixel row,

the second, fourth, and fifth pixels of the first pixel row are electrically connected to the second gate line located at the second side of the first pixel row,

a (j-1)-th stage (j is a natural number) which is formed in a second peripheral area of the display area opposite to the first peripheral area and provides a gate signal to the second gate line of the first pixel row;

a j-th stage which is formed in the second peripheral area adjacent to the (j-1)-th stage and provides a gate signal to the second gate line of the second pixel row, and

a first discharging transistor which is formed in the second peripheral area between the (j-1)-th stage and the j-th stage and discharges a high voltage applied to the first gate line of the second pixel row to a low voltage, wherein

the first discharging transistor does not overlap the second discharging transistor in the row direction."

2 Summary of the reasons for refusal by the body

(1) Reason 1 (New matter)

It cannot be said that the matter, "first discharging transistor does not overlap the second discharging transistor in the row direction", described in Claim after the First amendment, is a matter described in the Specification, the Scope of Claims, or drawings originally attached to the Application.

Therefore, the First amendment, which does not fall within the scope of the matter described in the Specification, the Scope of Claims, or drawings originally attached to the Application, does not satisfy the requirements stipulated in Article 17-2(3) of the Patent Act.

(2) Reason 2 (Inventive step)

The Invention could have been easily made by a person skilled in the art based on the inventions described in Cited Documents 1 to 4, and Cited Documents 6 and 7. Thus, the appellant should not be granted a patent for the invention under the provisions of Article 29(2) of the Patent Act.

Cited Document 1: Japanese Unexamined Patent Application Publication No. 2009-151258

Cited Document 2: U.S. Patent Application Publication No. 2010/0156954 Specification

Cited Document 3: Japanese Unexamined Patent Application Publication No. 2010-20279

Cited Document 4: Japanese Unexamined Patent Application Publication No. 2007-72463

Cited Document 6: Japanese Unexamined Patent Application Publication No. 2006-337710

Cited Document 7: Japanese Unexamined Patent Application Publication No. 2005-122183

3 Regarding Reason 1 (New matter)

Claim 1 after the First amendment includes the description, "the first discharging transistor does not overlap the second discharging transistor in the row direction".

However, no description regarding the matter can be found in the Specification, the Scope of Claims, or the drawings originally attached to the Application (hereinafter referred to as "Originally attached description, etc.").

We will examine the allegation of the appellant in the First written opinion that the matter is based on the descriptions in [0073] to [0079] etc., and FIG. 12 of the Originally attached Description, etc.

(1) Description of the Originally attached Description, etc.

The descriptions in [0073] to [0079] and FIG. 12 of the Originally attached Description, etc. are as follows. The underlines were added by the body.

"[0073]

FIG. 12 is a conceptual diagram illustrating a display panel of another exemplary embodiment of the invention.

Referring to FIG. 1, FIG. 4, and FIG. 12, the display panel 600 of this embodiment includes the second and first discharging circuits 242, 241 in addition to the first and second gate driving circuits 210, 230 in the first and second peripheral areas PA1, PA2.

[0074]

The first gate driving circuit 210 includes a plurality of stages (SCi-1, SCi) formed in a first peripheral area PA1, and each of the stages provides a gate signal to gate lines (GLi-1, GLi) arranged at the first side of one pixel row. The first gate driving circuit 210 is electrically connected to one end of the gate lines (GLi-1, GLi) on the side of the first peripheral area PA1.

[0075]

The first discharging circuit 241 is formed in a second peripheral area PA2. The first discharging circuit 241 is electrically connected to a gate line at the first side of each pixel row, and discharges a high voltage VON of the gate signal applied to the gate line to a low voltage VOFF. The first discharging circuit 241 includes a first discharging transistor TR1 and a voltage line VL with the low voltage VOFF applied thereto. As shown in the figure, the first discharging transistor TR1 is formed in the second peripheral area PA2 between the stages (SCj-1 and SCj) and is formed in the second peripheral area PA2 corresponding to a width of the pixel row defined by the (i-1)-th and (j-1)-th gate

lines GLi-1 and GLj-1.

[0076]

The first discharging transistor TR1 includes a first control electrode, a first input electrode, and a first output electrode. The first control electrode is connected to the i-th gate line GLi connected to the i-th stage SCi, the first input electrode is connected to the (i−1)-th gate line GLi-1, and the first output electrode is connected to the voltage line VL. When the high voltage VON is applied to the i-th gate line GLi, the first discharging transistor TR1 is turned on and discharges the high voltage VON applied to the (i-1)-th gate line GLi-1 to the low voltage VOFF.

[0077]

The second gate driving circuit 230 includes the stages (SCj-1, SCj) formed in the first peripheral area PA1, and each of the stages provides the gate signals to the gate lines (GLj-1, GLj) arranged at the second side of each pixel row. The second gate driving circuit 230 is electrically connected to one end of the gate lines (GLj-1, GLj) on the side of the second peripheral area PA2.

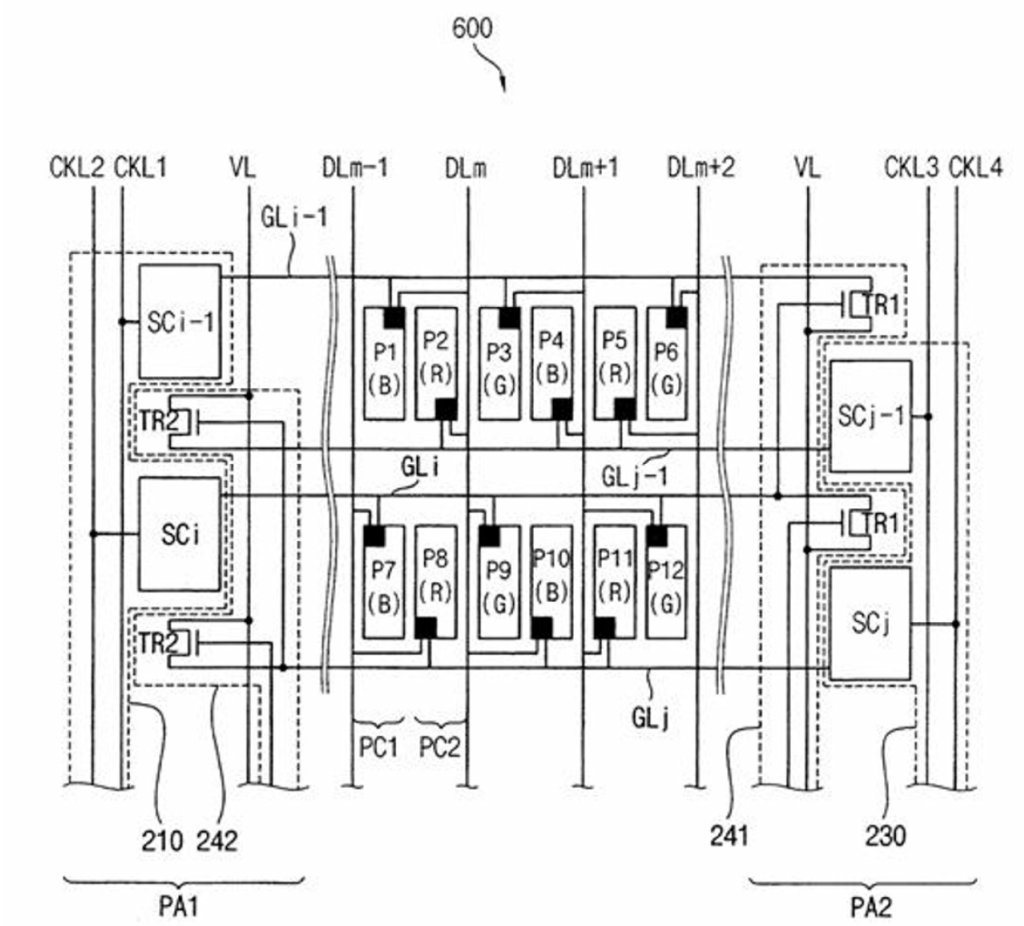
[0078]

The second discharging circuit 242 is formed in the first peripheral area PA1. The second discharging circuit 242 is electrically connected to the gate line at the second side of each pixel row, and discharges the high voltage VON of the gate signal applied to each gate line to the low voltage VOFF. The second discharging circuit 242 includes a second discharging transistor TR2 and a voltage line VL with the low voltage VOFF applied thereto. As shown in the figure, the second discharging transistor TR2 is formed in the first peripheral area PA1 between the stages (SCi-1, SCi) and is formed in the first peripheral area PA1 corresponding to the width of the pixel row defined by the (i-1)-th and (j-1)-th gate lines GLi-1 and GLj-1.

[0079]

The second discharging transistor TR2 includes a second control electrode, a second input electrode, and a second output electrode. For example, the second control electrode is connected to the j-th gate line GLj connected to the j-th stage SCj, the second input electrode is connected to the (j-1)-th gate line GLj-1, and the second output electrode is connected to the voltage line VL. When the high voltage VON is applied to the j-th gate line GLj, the second discharging transistor TR2 is turned on and discharges the high voltage VON applied to the (j-1)-th gate line GLj-1 to the low voltage VOFF."

"[FIG. 12]



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(2) Judgment

A According to the descriptions (especially, underlined parts) in (1) of the Originally attached Description, etc., the following matters are acknowledged regarding formation of the first discharging transistor TR1 and the second discharging transistor TR2.

(A) The stage SCi-1 and the stage SCi are formed in the first peripheral area PA1 ([0074]), and the second discharging transistor TR2 is formed between the stage SCi-1 and the stage SCi ([0078]).

In the same way, the stage SCj-1 and the stage SCj are formed in the second peripheral area PA2 ([0077]), and the first discharging transistor TR1 is formed between the stage SCj-1 and the stage SCj ([0075]).

Meanwhile, the description, "the stages (SCj-1, SCj) formed in the first peripheral area PA1" ([0077]), is obviously an error for the description, "the stages (SCj-1, SCj) formed in the second peripheral area PA2", in light of a comparison with the description,

"a plurality of stages (SCi-1, SCi) formed in a first peripheral area PA1" ([0074]), and positional relationship between the symbols, "SCj-1", "SC", and "PA2" shown in FIG. 12.

(B) The first discharging transistor TR1 is formed in the second peripheral area PA2 corresponding to a width of the pixel row defined by the (i-1)-th and (j-1)-th gate lines GLi-1 and GLj-1 ([0075]).

In the same way, the second discharging transistor TR2 is formed in the first peripheral area PA1 corresponding to the width of the pixel row defined by the (i-1)-th and (j-1)-th gate lines GLi-1 and GLj-1 ([0078]).

B First, according to A (A), the position where the second discharging transistor TR2 is formed, is specified by the relationship between the stage SCi-1 and the stage SCi formed in the first peripheral area PA1. In the same way, the position where the first discharging transistor TR1 is formed, is specified by the relationship between the stage SCj-1 and the stage SCj formed in the second peripheral area PA2.

However, the positional relationship between the stages SCi-1 and SCi formed in the first peripheral area PA1 and the stages SCj-1 and SCj formed in the second peripheral area PA2 is not described in the Originally attached Description, etc.

Therefore, even if the position of the second discharging transistor TR2 is specified by the relationship between the stages SCi-1 and SCi and the position of the first discharging transistor TR1 is specified by the relationship between the stages SCj-1 and SCj, the positional relationship between the second discharging transistor TR2 and the first discharging transistor TR1 is not specified at all.

Thus, it cannot be said that the first discharging transistor TR1 does not overlap the second discharging transistor TR2 in the row direction, based on A (A).

C Next, according to A (B), the first discharging transistor TR1 and the second discharging transistor TR2, which are formed in the second peripheral area PA2 and the first peripheral area PA1 respectively, are formed in peripheral areas corresponding to the width of the pixel row defined by the (i-1)-th and (j-1)-th gate lines GLi-1 and GLj-1.

Examining the description, "formed in peripheral areas corresponding to the width of the pixel row defined by the (i-1)-th and (j-1)-th gate lines GLi-1 and GLj-1", based on the description in the Originally attached Description, etc., the description means as follows: "the first stage and the second discharging transistor may be formed in the first peripheral area so as to have a width smaller than or equal to a width of a pixel row defined by the first and second gate lines, and the second stage and the first discharging

transistor may be formed in the second peripheral area so as to have a width smaller than or equal to the width of the pixel row" ([0008]).

(A) The object of the invention according to the Application is to solve the following problem: when employing a structure where two pixels adjacent to each other share one data line, the number of data driving circuits can be reduced, while two circuit stages are required for generating two gate signals required for driving one pixel row, resulting in increasing an area of the peripheral area forming the circuit stages and increasing a bezel width of the display apparatus ([0003], [0004], [0006]).

(B) The invention according to the Application is to solve the problem in (A) by providing a first gate line at the first side of one pixel row and a second gate line at the second side, and providing a first gate driving circuit including a first stage to provide a gate signal to the first gate line, in the first peripheral area, and a second gate driving circuit including a second stage to provide a gate signal to the second gate line, in the second peripheral area ([0008], [0011]).

(C) The first stage and the second stage are formed in the first peripheral area and the second peripheral area, respectively, so as to have a width smaller than or equal to a width of a pixel row defined by the first and second gate lines ([0008]).

The reason for the requirements on the width of the first stage and the width of the second stage is not described in the Originally attached Description, etc.

However, in light of the fact that both first and second gate driving circuits include a plurality of stages cascade-connected to each other ([0020], [0022]), it is recognized that the reason of the requirements on the width of the first stage and the width of the second stage is that a plurality of first stages and a plurality of second stages are to be arranged in a row in the first peripheral area and the second peripheral area, respectively. If the width of the first stage and the width of the second stage are larger than the pixel row width, multiple first stages and multiple second stages cannot be arranged in a row in the first peripheral area and the second peripheral area, respectively. This is contrary to the object of the invention according to the Application (the above (A)) which is to solve the problem that a bezel width of the display apparatus is increased.

As a specific configuration thereof, in the embodiment described in [0014] to [0042], FIG. 1 and FIG. 4 of the Originally attached Description, etc., both width W1 of the (i-1)-th stage SCi-1 and the i-th stage SCi of the first gate driving circuit and width W1 of the (j-1)-th stage SCj-1 and the j-th stage SCj of the second gate driving circuit are

configured not to be larger than the width W2 of the pixel row (first pixel row PL1, second pixel row PL2) defined by two gate lines ([0020] and [0023]).

(D) When the first discharging circuit including the first discharging transistor and the second discharging circuit including the second discharging transistor are included in addition to the first gate driving circuit and the second gate driving circuit, "the first stage and the second discharging transistor may be formed in the first peripheral area so as to have a width smaller than or equal to a width of a pixel row defined by the first and second gate lines, and the second stage and the first discharging transistor may be formed in the second peripheral area so as to have a width smaller than or equal to the width of the pixel row" ([0008]).

The reason for the requirements on the width of the first stage and the second discharging transistor and the width of the second stage and the first discharging transistor is not described in the Originally attached Description, etc.

However, in light of the fact that both first and second gate driving circuits include a plurality of stages cascade-connected to each other and the discharging transistor is formed between two stages ([0074], [0075], [0077], [0078]), it is recognized that the reason for the requirements on the width of the first stage and the second discharging transistor and the width of the second stage and the first discharging transistor is the same as that described in (C). Therefore, the reason is that a plurality of first stages and the second discharging transistor formed between them are to be arranged in a row in the first peripheral area and a plurality of second stages and the first discharging transistor formed between them are to be arranged in a row in the second peripheral area.

As a specific configuration thereof, in the embodiment described in [0073] to [0079] and FIG. 12 of the Originally attached Description, etc., as described in A (B), it is acknowledged that both a first discharging transistor TR1 and a second discharging transistor TR2 are formed in peripheral areas corresponding to the pixel row width defined by the (i-1)-th and (j-1)-th gate lines GLi-1, GLj-1 ([0075], [0078]).

Thus, it is reasonable to recognize that the description, "formed in peripheral areas corresponding to the width of the pixel row defined by the (i-1)-th and (j-1)-th gate lines GLi-1 and GLj-1" means that "the first stage and the second discharging transistor may be formed in the first peripheral area so as to have a width smaller than or equal to a width of a pixel row defined by the first and second gate lines, and the second stage and the first discharging transistor may be formed in the second peripheral area so as to have a width smaller than or equal to the width of the pixel row" ([0008]).

D According to A (B), the positional relationship between the first discharging transistor TR1 and the second discharging transistor TR2 is not specified at all, only by the fact that the width of the first discharging transistor TR1 and the second discharging transistor TR2 is specified by the relationship with the width of the pixel row defined by the (i-1)-th and (j-1)-th gate lines GLi-1 and GLj-1.

Therefore, it cannot be said, based on A (B), that the first discharging transistor TR1 and the second discharging transistor TR2 do not overlap each other in the row direction.

E Apart from the description of the Originally attached Description, etc., even if we recognize that it is specified that both the first discharging transistor TR1 and the second discharging transistor TR2 are located inside the pixel row defined by the (i-1)-th and (j-1)-th gate lines GLi-1 and GLj-1, based on A (B), the positions in the width direction of the first discharging transistor TR1 and the second discharging transistor TR2 are not specified. Thus, it still cannot be said that the transistors do not overlap each other in the row direction.

F Referring to FIG. 12 of the Originally attached Description, etc., the "first discharging transistor TR1" and the "second discharging transistor TR2" do not overlap each other in the row direction (lateral direction in FIG. 12), apparently.

However, in general, since a drawing attached to a patent application is an explanatory drawing that complements the contents described in the Specification and allows a person skilled in the art to comprehend the technical content regarding an invention for which a patent is sought, it is enough so long as the drawing has accuracy required for comprehending the technical content of the invention. The drawing does not necessarily have accuracy required for a design drawing regarding the size and arrangement of members.

The invention according to the Application is, when employing a structure where two adjacent pixels share one data line, to solve the problem that a bezel width of the display apparatus is increased, by arranging the first gate driving circuit including the first stage that provides a gate signal to the first gate line, in the first peripheral area, and arranging the second driving circuit including the second stage that provides a gate signal to the second gate line, in the peripheral area (the above C (A) and (B)).

Thus, it is recognized that the first gate driving circuit 210 is arranged in the first peripheral area PA1 and the second driving circuit 230 is arranged in the second peripheral area PA2 from FIG. 12, which is a "conceptual diagram illustrating a display

panel of another exemplary embodiment of the invention" ([0073]). However, we should not recognize technical matters which do not directly relate to the problem of the invention and means for solving the problem according to the Application as to whether the first discharging transistor TR1 and the second discharging transistor TR2 overlap each other in the row direction.

Therefore, it cannot be said, based on FIG. 12, that the first discharging transistor TR1 and the second discharging transistor TR2 do not overlap each other in the row direction.

G As described above, it cannot be said that the first discharging transistor TR1 and the second discharging transistor TR2 do not overlap each other in the row direction from the descriptions in [0073] to [0079] and FIG. 12 of the Originally attached Description, etc.

(3) Summary of Reason 1

As described above, it cannot be said that the first discharging transistor TR1 and the second discharging transistor TR2 do not overlap each other in the row direction from the descriptions in [0073] to [0079] and FIG. 12 of the Originally attached Description, etc. No description is found about the fact that the first discharging transistor TR 1 and the second discharging transistor TR2 do not overlap each other, in other parts of the Originally attached Description, etc.

Therefore, it cannot be said that the matter described in Claim 1 after the First amendment, "the first discharging transistor does not overlap the second discharging transistor in the row direction", does not introduce a new technical matter in relation to the technical matters derived by integrating all descriptions in the Originally attached Description, etc.

Thus, the First amendment, which does not fall within the scope of the matter described in the Originally attached Description, etc., does not satisfy the requirements stipulated in Article 17-2(3) of the Patent Act.

4 Regarding Reason 2 (Inventive step)

(1) Invention described in Cited Document 1

A Cited Document 1 includes the following descriptions. The underlines were added by the body.

(A) Embodiment 1

"[0014]

(Embodiment 1)

FIG. 2 is a block diagram of an image display device according to this embodiment. The image display device shown in FIG. 2 is illustrated as a liquid display device which drives pixels by a TFT. The image display device according to this invention is not limited to a liquid display device, and can be applied to an organic EL display device, or the like, having the same configuration.

[0015]

A pixel array 1 shown in FIG. 2 comprises m x n pixels 4, and each of the pixels is driven by the TFT. The first gate line (the top line in the figure) of the pixel array 1 is G1, the last gate line (the bottom line in the figure) is Gn, the leftmost source line is S1, and the rightmost source line is Sm.

[0016]

The first gate driver circuit 2 shown in FIG. 2 comprises shift register circuits SRCO1-SRCOn which scan odd gate lines from the start gate line G1 to the end gate line Gn-1. The first gate driver circuit 2 is formed of an amorphous silicon TFT.

... (Omitted) ...

[0018]

The second gate driver circuit 3 shown in FIG. 2 comprises shift register circuits SRCE2-SRCEn+1 which scan even gate lines from the start gate line G2 to the end gate line Gn. The second gate driver circuit 3 is formed of an amorphous silicon TFT.

... (Omitted) ...

[0020]

The source driver circuit 5 shown in FIG. 2 switches output polarity in synchronization with a source polarity control signal POL, and switches a source signal based on image data DATA (including a control signal) in synchronization with a source switching control signal SSEL. The source driver circuit 5 is connected to source lines S1-Sm, and a source signal is provided to each of the source lines S1-Sm.

[0021]

The timing generation circuit 6 shown in FIG. 2 comprises gate driver control signal generation circuits 7, 8 which generate gate driver control signals on the basis of a vertical synchronization signal, a horizontal synchronization signal, a dot clock signal, and a data enable signal. The gate driver control signals include start signals STVO, STVE, and clock signals CKVO, CKVBO,CKVE, CKVBE. The gate driver control signal generation circuit 7 is provided with a delay amount setting signal to adjust output timing.

... (Omitted) ...

[0023]

The first gate driver circuit 2 and the second gate driver circuit 3 comprise multi-stage shift register circuits that sequentially output gate signals SROUT1-n to each of the gate lines. Each shift register circuit in the stages activates a gate potential of a transistor (not shown) driving a gate line in synchronization with a gate signal output from a shift register circuit in the previous stage, to output a gate signal in synchronization with a clock signal. On the basis of a gate signal output from the subsequent stage, the transistor driving a gate line is reset. In FIG. 2, supplied gate signals which are output from the subsequent stages are omitted.

[0024]

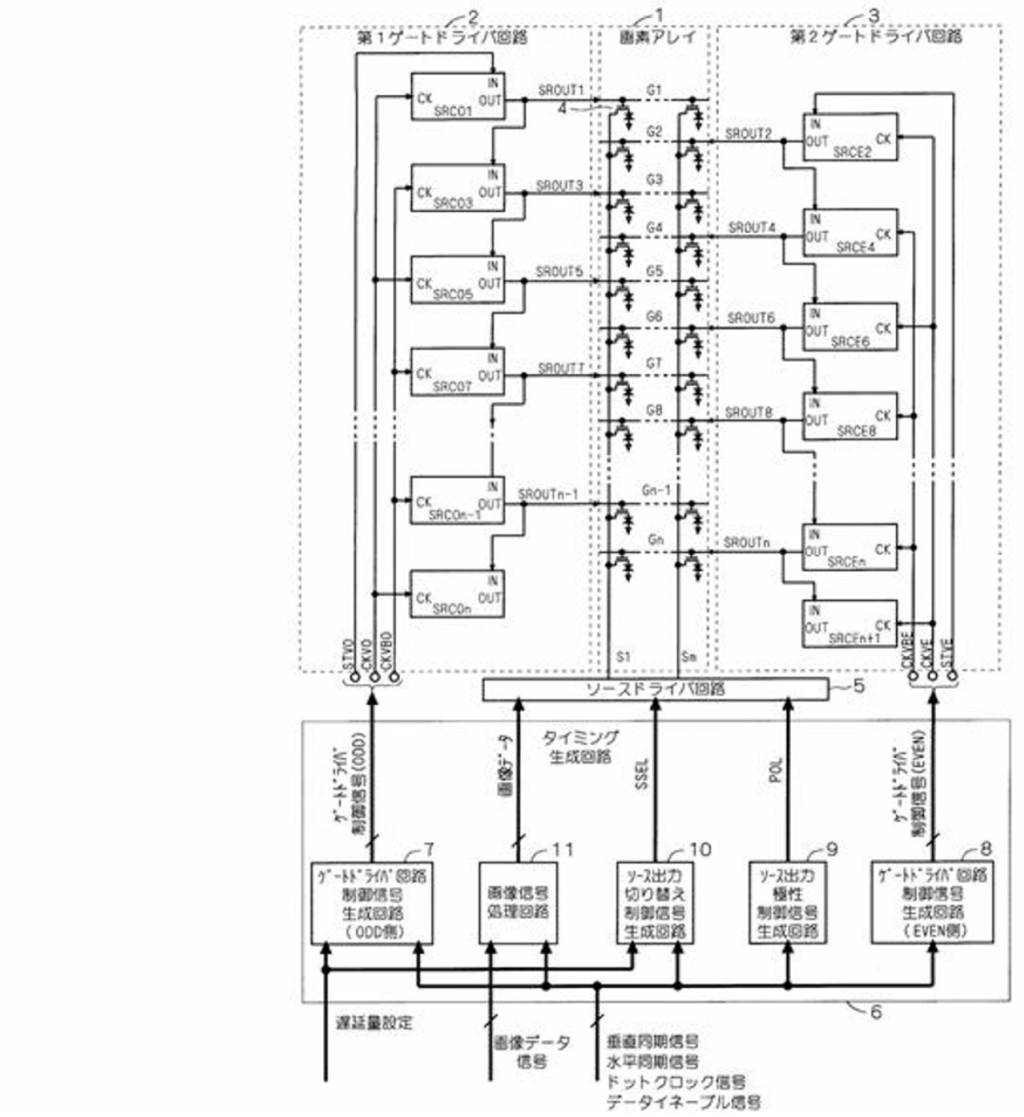
The image display device shown in FIG. 2 is configured to arrange the first and second gate driver circuits 2, 3 on both sides of the pixel array 1. This invention is not limited to this arrangement. The first and second gate driver circuits 2, 3 may be arranged on opposite side or may be arranged on only one side, so long as the connection is the same. In FIG. 2, power sources VDD, VSS supplied to the shift register circuits are omitted. In this invention, the presence of the power source VDD does not matter. In the block diagram shown in FIG. 2, a power source circuit for supplying power source voltage to circuits and a level shift circuit for converting a voltage level to drive a gate driver circuit are omitted.

... (Omitted) ...

[0033]

The first and second gate driver circuits 2, 3 are operated by overlap scanning which is the same method as disclosed in Patent Document 1, basically. Specifically, in the image display device shown in FIG. 2, the first gate driver circuit 2 on the left side drives odd gate lines G1, G3, G5 ..., the second gate driver circuit 3 on the right side drives even gate lines G2, G4, G6 ...."

"[FIG. 2]



第１ゲートドライバ回路　First gate driver circuit

画素アレイ　Pixel array

第２ゲートドライバ回路　Second gate driver circuit

ソースドライバ回路　Source driver circuit

ゲートドライバ制御信号（ＯＤＤ）　Gate driver control signal (ODD)

画像データ　Image data

タイミング生成回路　Timing generation circuit

ゲートドライバ制御信号（ＥＶＥＮ）　Gate driver control signal (EVEN)

ゲートドライバ回路制御信号生成回路（ＯＤＤ側）　Gate driver circuit control signal generation circuit (ODD-side)

画像信号処理回路　Image signal processing circuit

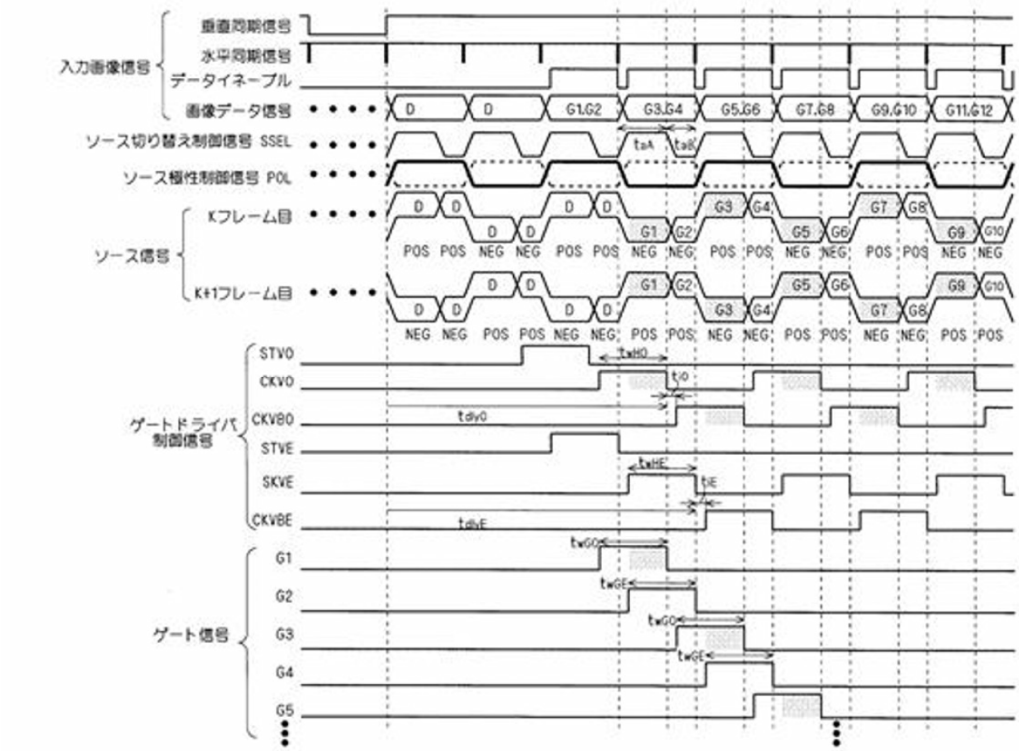
ソース出力切り替え制御信号生成回路　Source output switching control signal generation circuit

ソース出力極性制御信号生成回路　Source output polarity control signal generation circuit
ゲートドライバ回路制御信号生成回路（ＥＶＥＮ側）　Gate driver circuit control signal generation circuit (EVEN-side)
遅延量設定　Delay amount setting
画像データ信号　Image data signal
垂直同期信号　Vertical synchronization signal
水平同期信号　Horizontal synchronization signal
ドットクロック信号　Dot clock signal
データイネーブル信号　Data enable signal

"

(B) Embodiment 2
"[0042]
(Embodiment 2)
In this embodiment, unlike Embodiment 1, the image display device having pixel arrangement shown in FIG. 5 is driven by the timing chart shown in FIG. 4. The image display device according to this embodiment includes, as shown in FIG. 5, two gate lines with respect to pixels in the same row. Specifically, RGB pixels in the first row in FIG. 5 are connected to the gate line G1 (SP2, 4, 6) or connected to the gate line G2 (SP1, 3, 5). Thus, the gate lines are twice as many as those having the pixel arrangement shown in FIG. 3, while the source lines are reduced to half.
... (Omitted) ...
[0044]
Other timings are as shown in the timing chart in FIG. 1, and a configuration of the image display device according to this embodiment is the same as the configuration shown in FIG. 2. The driving method according to this embodiment is implemented by applying the driving method of Embodiment 1 to the driving method disclosed in Non-patent Document 2. Details regarding the parts overlapping Embodiment 1 and Non-patent Document 2 are omitted."

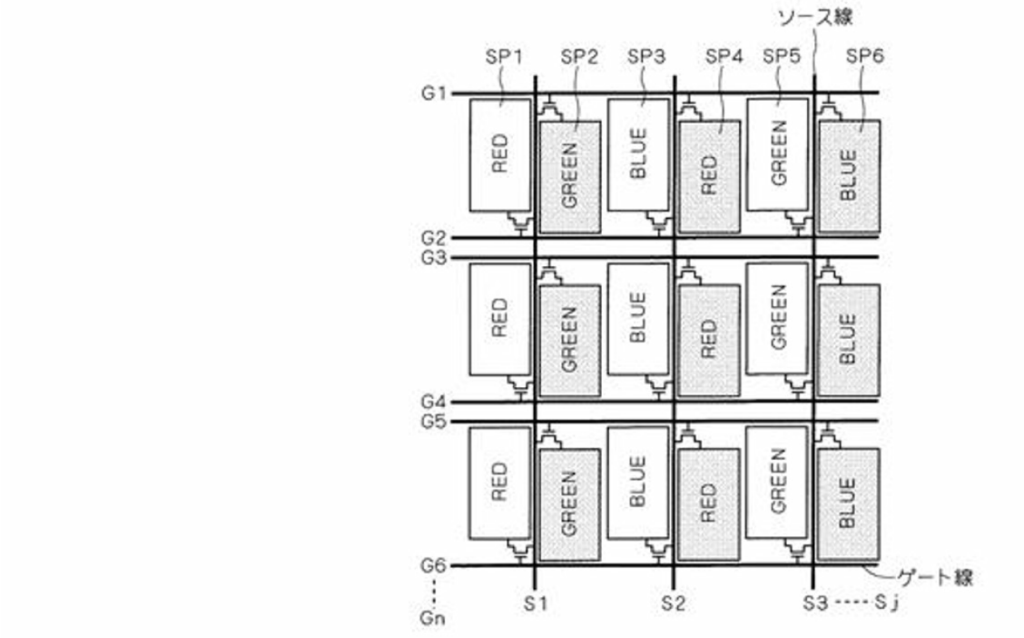
"[FIG. 4]



入力画像信号　Input image signal
垂直同期信号　Vertical synchronization signal
水平同期信号　Horizontal synchronization signal
データイネーブル　Data enable
画像データ信号　Image data signal
ソース切り替え制御信号　Source switching control signal
ソース極性制御信号　Source polarity control signal
ソース信号　Source signal
フレーム目　-th frame
ゲートドライバ制御信号　Gate driver control signal
ゲート信号　Gate signal

"

"[FIG. 5]



ソース線　　Source line
ゲート線　　Gate line

"

(C) Embodiment 3

"[0048]

(Embodiment 3)

In the driving method disclosed in Non-patent Document 2, there is no source switching control signal SSEL as shown in the timing chart in FIG. 9, and the source signal always has the same output period. When a source signal in the (n-i)-th line and a source signal in the n-th line are opposite in polarity, pixels are insufficiently charged. In the image display device according to this embodiment, degradation of display quality due to insufficient charge is prevented by intentionally selecting the color of the pixel which is insufficiently charged due to opposite polarity between the source signal in the (n-1)-th line and the source signal in the n-th line.

[0049]

Specifically, FIG. 7 and FIG. 8 illustrate m x n pixel arrangement and connection of source lines and gate lines of the image display device according to the embodiment. In the pixel arrangement shown in FIG. 7, green pixels SP2, 5 connected to the source lines S1, S3 and a blue pixel SP3 connected to the source line S2 are connected to odd gate lines G1, G3, G5. In the pixel arrangement shown in FIG. 7, red pixels SP1, 4

connected to the source lines S1, S2 and a blue pixel SP6 connected to the source line S3 are connected to the even gate lines G2, G4, G6.

[0050]

In the pixel arrangement shown in FIG. 7, when the pixels are driven by the timing chart shown in FIG. 9, a pixel connected to an odd gate line is insufficiently charged. Thus, in the pixel arrangement shown in FIG. 7, only half of the green and blue pixels are insufficiently charged, and the red and the other half of the blue pixels are not charged.

[0051]

Generally, when color shading is generated in the same color, pixels insufficiently charged are visually recognized as reduction in display quality. When only subpixels are insufficiently charged, color shading is not generated while chromaticity is changed, and the insufficient charging is not visually recognized. In the pixel arrangement shown in FIG. 5, color shading is generated in all of red, green, and blue colors. In the pixel arrangement shown in FIG. 7, color shading is generated only in blue color, having lowest luminosity, thereby preventing reduction in display quality which would otherwise occur due to visual recognition of insufficiently charged pixels. The change in chromaticity caused by the pixel arrangement shown in FIG. 7 can be predicted and improved by adjusting reference voltage of the source driver circuit 5, thereby providing higher display performance.

[0052]

In this embodiment, the pixel arrangement shown in FIG. 7 is presented as a method of preventing reduction in display quality due to insufficiently charged pixels. This invention can employ not only the pixel arrangement shown in FIG. 7 but also the pixel arrangement shown in FIG. 8. In the pixel arrangement shown in FIG. 8, red pixels SP1, 4 connected to the source lines S1, S2 and a blue pixel SP6 connected to the source line S3 are connected to odd gate lines G1, G3, G5. In the pixel arrangement shown in FIG. 8, green pixels SP2, 5 connected to the source lines S1, S3 and a blue pixel SP3 connected to the source line S2 are connected to even gate lines G2, G4, G6. In the pixel arrangement shown in FIG. 8, only half of the red and blue pixels are insufficiently charged, and the green and the other half of the blue pixels are not charged. Thus, the same effect as that in the pixel arrangement shown in FIG. 7 can be obtained.

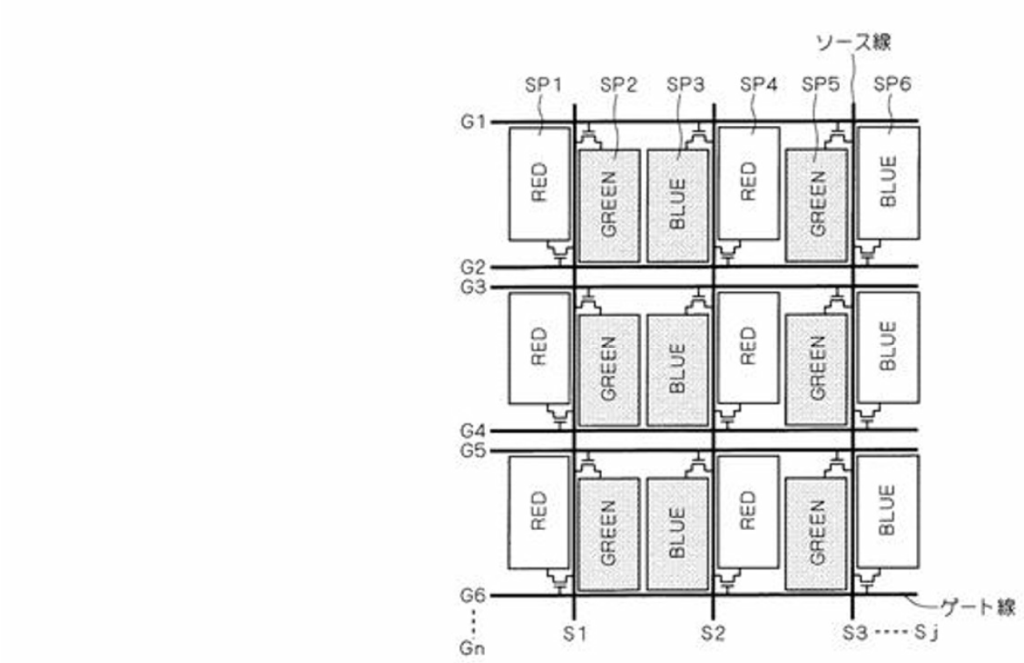
[0053]

As described above, the image display device according to the embodiment, which employs pixel arrangements shown in FIG. 7 and FIG. 8, has an effect of preventing reduction in display quality (color shading) due to insufficiently charged pixels.

[0054]

By employing the driving method described in Embodiment 2 to the image display device according to the embodiment, an effect of preventing reduction in circuit operation margin can be obtained while preventing insufficient charging. Specifically, the image display device employing the pixel arrangements shown in FIG. 7 and FIG. 8 can be driven by the timing chart shown in FIG. 4."

"[FIG. 7]



ソース線　　Source line
ゲート線　　Gate line

"

B　According to the description of A in Cited Document 1, the following matters are acknowledged. (A) FIG. 2, which is a block diagram ([0014]) of the image display device according to Embodiment 1, illustrates that m x n pixels 4 are arranged in the pixel array 1, each of the pixels is driven by the TFT, and the first (top) gate line in the pixel array 1 is G1, the last (bottom) gate line is Gn, the leftmost source line is S1, and the rightmost source line is Sm ([0015]).

In light of the above, according to FIG. 7 ([0049]) illustrating m x n pixel arrangement and connection of source lines and gate lines of the image display device according to Embodiment 3, it is recognized that FIG. 7 shows a "pixel array including

pixels in multiple rows and multiple columns corresponding to n gate lines G1 to Gn extending in the row direction and j source lines S1 to Sj extending in the column direction, each of the pixels being driven by the TFT".

(B) In addition, it is recognized from FIG. 7 that "red, green, and blue pixels in each row of the pixel array are sequentially arranged from the left, each set of two of the n gate lines G1 to Gn is associated with one row of the pixels, one of the j source lines S1 to Sj is associated with two columns of the pixels, two rows of pixels associated with one source line are arranged on both sides (row direction) of the one source line, and one row of pixels associated with two gate lines is sandwiched vertically (column direction) by the two gate lines and connected to one of the two gate lines".

(C) Embodiment 2 is different in timing chart and pixel arrangement from Embodiment 1 ([0042]). However, the configuration of the image display device is the same as the configuration shown in FIG. 2 (Embodiment 1) ([0044]). Thus, it is recognized that the "first gate driver circuit 2", the "second gate driver circuit 3", the "source driver circuit 5", and the "timing generation circuit 6" are comprised in the same way as in Embodiment 1. (FIG. 2).

(D) Embodiment 3 can employ the driving method described in Embodiment 2; specifically, the image display device employing the pixel arrangement shown in FIG. 7 can be driven by the timing chart shown in FIG. 4 ([0054]). Thus, it is recognized that the configuration for driving of Embodiment 3 is the same as that of Embodiment 2. The configuration comprises the "first gate driver circuit 2", the "second gate driver circuit 3", the "source driver circuit 5", and the "timing generation circuit 6" in the same way as in Embodiment 1 (the above (C)).

Therefore, the image display device according to Embodiment 3, which is an image display device employing the pixel arrangement shown in FIG. 7, comprises, as a configuration for driving, the "first gate driver circuit 2", the "second gate driver circuit 3", the "source driver circuit 5", and the "timing generation circuit 6" in the same way as in Embodiment 1, and is driven by the timing chart shown in FIG. 4.

(E) In light of the above, according to the description of A in Cited Document 1, Cited Document 1 describes the following invention (hereinafter referred to as "Cited Invention") as Embodiment 3.

"An image display device which drives pixels by a TFT ([0014]), comprising:

a pixel array comprising pixels in multiple rows and multiple columns corresponding to n gate lines G1 to Gn extending in the row direction and j source lines S1 to Sj extending in the column direction, each of the pixels being driven by the TFT ((A));

a first gate driver circuit 2 arranged on the left side of the pixel array and comprising shift register circuits SRCO1-SRCOn which scan odd gate lines from the start gate line G1 to the end gate line Gn-1 ([0024], [0033], [0016]);

a second gate driver circuit 3 arranged on the right side of the pixel array and comprising shift register circuits SRCE2-SRCEn+1 which scan even gate lines from the start gate line G2 to the end gate line Gn ([0024], [0033], [0018]);

a source driver circuit 5 connected to source lines S1-Sj and supplying a source signal to each of the source lines S1-Sj ([0020], FIG. 7, the above (A)); and

a timing generation circuit 6 which generates a gate driver control signal ([0021]), wherein

each shift register circuit in the first gate driver circuit 2 and the second gate driver circuit 3 activates a gate potential of a transistor driving a gate line in synchronization with a gate signal output from a shift register circuit in the previous stage, to output a gate signal in synchronization with a clock signal, and, on the basis of a gate signal output from the subsequent stage, the transistor driving a gate line is reset ([0023]),

red, green, and blue pixels in each row of the pixel array are sequentially arranged from the left, each set of two of the n gate lines G1 to Gn is associated with one row of the pixels, one of the j source lines S1 to Sj is associated with two columns of the pixels, two columns of pixels associated with one source line are arranged on both sides (row direction) of the one source line to be connected to the one source line, and one row of pixels associated with two gate lines is sandwiched vertically (column direction) by the two gate lines and connected to one of the two gate lines (the above (B)),

green pixels SP2, 5 connected to the source lines S1, S3 and a blue pixel SP3 connected to the source line S2 are connected to odd gate lines G1, G3, G5, and red pixels SP1, 4 connected to the source lines S1, S2 and a blue pixel SP6 connected to the source line S3 are connected to the even gate lines G2, G4, G6 ([0049], FIG. 7)."

(2) Comparison

The Invention and the Cited Invention are compared as follows.

A The combination of

the "pixel array comprising pixels in multiple rows and multiple columns corresponding to n gate lines G1 to Gn extending in the row direction and j source lines S1 to Sj extending in the column direction, each of the pixels being driven by the TFT",
the "first gate driver circuit 2 comprising shift register circuits SRCO1-SRCOn which scan odd gate lines from the start gate line G1 to the end gate line Gn-1", and
the "second gate driver circuit 3 comprising shift register circuits SRCE2-SRCEn+1 which scan even gate lines from the start gate line G2 to the end gate line Gn" in the "image display device which drives pixels by a TFT" of the Cited Invention

corresponds to the "display panel" of the Invention.

B The "pixels in multiple rows and multiple columns" in the "pixel array" of the Cited Invention

correspond to "a plurality of pixels arranged in a display area and including a first pixel row and a second pixel row" of the Invention.

C The "j source lines S1 to Sj extending in the column direction" which correspond to the "pixels in multiple rows and multiple columns" in the Cited Invention are configured so that "one source line is associated with two rows of pixels", and it is known as a matter of common general technical knowledge that there are four or more lines.

Thus, the above description corresponds to "an (m-1)-th data line, an m-th data line, an (m+1)-th data line, and an (m+2)-th data line (m is a natural number) which extend in a column direction and are arranged sequentially" in the Invention.

D The "n gate lines G1 to Gn extending in the row direction" which correspond to the "pixels in multiple rows and multiple columns" in the Cited Invention

correspond to "a plurality of gate lines which extend in a row direction" in the Invention.

E In the Cited Invention, "pixels" are arranged in "multiple rows" in the "pixel array", and "one row of pixels" is "sandwiched vertically (column direction) by the two gate lines".

In the same way as in the Invention, it can be said that "the first pixel row is arranged between a first gate line located at a first side of the first pixel row and a second gate line located at a second side of the first pixel row", and that "the second pixel row is arranged between a first gate line located at a first side of the second pixel row and a second gate line located at a second side of the second pixel row".

F The "left side of the pixel array" in the Cited Invention

corresponds to the "first peripheral area of the display area" in the Invention.

The adjacent two of the "shift register circuits SRCO1-SRCOn which scan odd gate lines from the start gate line to the end gate line" of the "first gate driver circuit 2" "arranged on the left side of the pixel array" in the Cited Invention

correspond to "an (i-1)-th stage (i is a natural number) which is formed in a first peripheral area of the display area and provides a gate signal to the first gate line of the first pixel row" and "an i-th stage which is formed in the first peripheral area adjacent to the (i-1)-th stage and provides a gate signal to the first gate line of the second pixel row".

G The "right side of the pixel array" in the Cited Invention

corresponds to the "second peripheral area of the display area opposite to the first peripheral area" in the Invention.

The adjacent two of the "shift register circuits SRCE2-SRCEn+1 which scan even gate lines from the start gate line to the end gate line" of the "second gate driver circuit 3" "arranged on the right side of the pixel array" in the Cited Invention

correspond to "a (j-1)-th stage (j is a natural number) which is formed in a second peripheral area of the display area opposite to the first peripheral area and provides a gate signal to the second gate line of the first pixel row" and "a j-th stage which is formed in the second peripheral area adjacent to the (j-1)-th stage and provides a gate signal to the second gate line of the second pixel row".

(3) Corresponding feature and Different features

According to the result of comparison described in (2), corresponding feature and different features between the Invention and the Cited Invention are as follows.

A Corresponding feature

"A display panel comprising:

a plurality of pixels arranged in a display area and comprising a first pixel row and a second pixel row;

a plurality of data lines including an (m-1)-th data line, an m-th data line, an (m+1)-th data line, and an (m+2)-th data line (m is a natural number) which extend in a column direction and are arranged sequentially;

a plurality of gate lines which extend in a row direction, wherein

the first pixel row is arranged between a first gate line located at a first side of the

first pixel row and a second gate line located at a second side of the first pixel row,

the second pixel row is arranged between a first gate line located at a first side of the second pixel row and a second gate line located at a second side of the second pixel row,

an (i-1)-th stage (i is a natural number) which is formed in a first peripheral area of the display area and provides a gate signal to the first gate line of the first pixel row; and

an i-th stage which is formed in the first peripheral area adjacent to the (i-1)-th stage and provides a gate signal to the first gate line of the second pixel row,

a (j-1)-th stage (j is a natural number) which is formed in a second peripheral area of the display area opposite to the first peripheral area and provides a gate signal to the second gate line of the first pixel row; and

a j-th stage which is formed in the second peripheral area adjacent to the (j-1)-th stage and provides a gate signal to the second gate line of the second pixel row."

B Different features

(A) Different Feature 1

The Invention includes the "a second discharging transistor which is formed in the first peripheral area between the (i-1)-th stage and the i-th stage and discharges a high voltage applied to the second gate line of the first pixel row to a low voltage" and "a first discharging transistor which is formed in the second peripheral area between the (j-1)-th stage and the j-th stage and discharges a high voltage applied to the first gate line of the second pixel row to a low voltage", and is configured so that "the first discharging transistor does not overlap the second discharging transistor in the row direction", whereas,

the Cited Invention does not include any discharging transistor.

(B) Different Feature 2

In the Invention, "first and second pixels in the first pixel row between the (m-1)-th data line and the m-th data line are electrically connected to the m-th data line", "third and fourth pixels in the first pixel row between the m-th data line and the (m+1)-th data line are electrically connected to the (m+1)-th data line", and "fifth and sixth pixels in the first pixel row between the (m+1)-th data line and the (m+2)-th data line are electrically connected to the (m+2)-th data line", whereas,

in the Cited Invention, "two columns of pixels associated with one source line are arranged on both sides (row direction) of the one source line to be connected to the one

source line".

(C) Different Feature 3

In the Invention, "the first, third, and sixth pixels of the first pixel row are electrically connected to the first gate line located at the first side of the first pixel row", and "the second, fourth, and fifth pixels of the first pixel row are electrically connected to the second gate line located at the second side of the first pixel row", whereas,

in the Cited Invention, "green pixels SP2, 5 connected to the source lines S1, S3 and a blue pixel SP3 connected to the source line S2", out of the "red, green, and blue pixels in each row" "arranged sequentially from the left" are connected to "odd gate lines G1, G3, G5", and "red pixels SP1, 4 connected to the source lines S1, S2 and a blue pixel SP6 connected to the source line S3" are connected to "even gate lines G2, G4, G6".

(4) Judgment on the Different Features

A Regarding Different Feature 1

Paragraphs [0001], [0006], [0020], [0022], and [0029] and FIG.1 of Cited Document 3 describe a technique of arranging, in a display device having a gate driver, shift registers with multiple driving stages adjacent to first end of gate lines, connecting a plurality of discharging transistors to second end of the gate lines, receiving a gate signal of the next gate line by control terminals of the driving stages and control electrodes of the discharging transistors, and discharging a corresponding gate line to a gate-off voltage, thereby normally resetting the driving stages.

On the other hand, the Cited Invention is an "image display device" comprising a "first gate driver circuit 2" and a "second gate driver circuit 3", and is configured so that "shift register circuits" are arranged at one end of a plurality of "gate lines", and "on the basis of a gate signal output from the subsequent stage, the transistor driving a gate line is reset".

Thus, a person skilled in the art could have easily conceived of employing the technique described in Cited Document 3 in order to normally reset the transistor for driving a gate line in the Cited Invention.

In this case, the "discharging transistors" are connected to ends of the gate lines which are opposite the ends where the "shift register circuits" are arranged, and the "discharging transistors" are arranged "on the right side of the pixel array" in order to discharge "odd gate lines" connected to the "shift register circuits SRCO1-SRCOn" "arranged on the left side of the pixel array". The "discharging transistors" are arranged "on the left side of the pixel array" in order to discharge "even gate lines" connected to

the "shift register circuits SRCE2-SRCEn+1" "arranged on the right side of the pixel array".

According to, for example, [0009], [0010], [0076], [0077], FIG. 6, and FIGS. 17-19 of Cited Document 6, [0012], [0013], and FIG. 1 of Cited Document 7, slim bezel design of a display device was a well-known problem before the priority date. In consideration of the above, in arranging "discharging transistors" on "the right side of the pixel array" and "the left side of the pixel array" in the Cited Invention, the idea of arranging the "discharging transistors" to be arranged "on the right side of the pixel array" between the "shift register circuits SRCE2-SRCEn+1" and arranging the "discharging transistors" to be arranged "on the left side of the pixel array" between the "shift register circuits SRCO1-SRCOn" is only a design matter which can be employed by a person skilled in the art appropriately. The idea that the "discharging transistors" are arranged on "the right side of the pixel array" and on "the left side of the pixel array" so as not to overlap each other in the row direction is also only a design matter which can be employed appropriately in examining optimal arrangement of members.

B Regarding Different Feature 2

For example, as shown in [0070] and FIG. 3 of Cited Document 2, and [0034] and FIG. 3 of Cited Document 4, as pixel arrangement where one source line is associated with two columns of pixels, a device in which both two pixels located between two source lines are connected to the right source line in one pixel row and both two pixels located between two source lines are connected to the left source line in the next pixel row had been well-known before the priority date.

In the Cited Invention, a person skilled in the art could have easily conceived of employing the well-known pixel arrangement in place of the pixel arrangement where "two columns of pixels associated with one source line are arranged on both sides (row direction) of the one source line to be connected to the one source line" to connect both of two pixels located between the source line Sm-1 and the source line Sm to the source line Sm.

C Regarding Different Feature 3

Cited Document 1 includes the following description regarding Embodiment 3 (i.e., Cited Invention): "In this embodiment, the pixel arrangement shown in FIG. 7 is presented as a method of preventing reduction in display quality due to insufficiently charged pixels. This invention can employ not only the pixel arrangement shown in FIG. 7 but also the pixel arrangement shown in FIG. 8" ([0052]). Thus, modification of pixel

arrangement of the Cited Invention is only a design matter which can be easily implemented by a person skilled in the art.

For example, in FIG. 7 of Cited Document 1 (the above (1) A (C)), if the source line "SP1" and the pixels "SP1" and "SP" connected thereto are omitted, the source lines "S2" and "S3" are renamed to "S1" and "S2", and the pixels "SP3", "SP4", "SP5", and "SP6" are renamed to "SP1", "SP2", "SP3", and "SP4", it is obvious that the pixels "SP1", "SP3" and "SP6" are connected to the gate line "G1" and the pixels "SP2", "SP4" and "SP5" are connected to the gate line "G2".

(5) Summary of Reason 2

As described above, the Invention could have been easily made by a person skilled in the art based on the invention described in Cited Document 1 (Cited Invention), the technology described in Cited Document 3, well-known problems described in Cited Documents 6 and 7, well-known pixel arrangement shown in Cited Documents 2 and 4, and the matters described in Cited Document 1. Therefore, the appellant should not be granted a patent under the provisions of Article 29(2) of the Patent Act.

5 Closing

The First amendment, which does not fall within the scope of the matter described in the Originally attached Description, etc., does not satisfy the requirements stipulated in Article 17-2(3) of the Patent Act.

Therefore, the present application should be rejected.

The Invention could have been easily made by a person skilled in the art based on the inventions described in Cited Documents 1 to 4 and Cited Documents 6 and 7. The appellant should not be granted a patent for the invention under the provisions of Article 29(2) of the Patent Act.

Thus, the present application should be rejected without examining inventions according to other claims.

Therefore, the appeal decision shall be made as described in the conclusion.

February 3, 2020

Chief administrative judge: NAKATSUKA, Naoki
Administrative judge: KOBAYASHI, Norifumi
Administrative judge: HAMANO, Takashi