Appeal Decision

Appeal No. 2020-1184

Appellant Tohoku University

Patent Attorney FUJIMOTO, Kenji

The case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2018-561112, entitled "SOLAR BATTERY" (International Publication No. WO2018/131060 published on July 19, 2018) has resulted in the following appeal decision.

Conclusion

The appeal of the case was groundless.

Reason

No. 1 History of the procedures

The application was originally filed on January 10, 2017 as an International Patent Application, and the history of the procedures is as follows.

July 2, 2019 : Submission of written amendment

Dated August 6, 2019 : Notification of reasons for refusal

October 7, 2019 : Submission of written opinion and written amendment

Dated October 23, 2019 : Examiner's decision of refusal

January 29, 2020 : Submission of written demand for appeal

March 9, 2020 : Submission of written amendment (formality) of written demand for appeal

Dated September 16, 2020 : Notification of reasons for refusal

November 11, 2020 : Submission of written opinion and written amendment

No. 2 Reasons for refusal

An outline of reasons for refusal notified by the body on September 16, 2020 is as follows.

The present application does not comply with the requirement under Article 36(6)(ii) of the Patent Act due to deficiencies in Claims 2 and 4 of the scope of claims in the point that it is unclear how the boundary of a "UV degradation preventing layer" and a "photovoltaic power generating layer" (immediately below it) is determined,

the present application does not comply with the requirement under Article 36(6)(i) of the Patent Act due to deficiencies in Claims 2 to 4 of the scope of claims in the point that the polarity of a fixed charge is not specified, and it cannot be said that the problem can be solved, and in the point that even if the polarity of the fixed charged is specified, it is not specified that the polarity of the "UV degradation preventing layer" is opposite to the polarity of the fixed charge, and

the inventions according to Claims 1 to 4 of the present application could have been easily made by a person ordinarily skilled in the field of the art, to which the invention belongs, prior to the application, on the basis of the invention described in the following Cited Document 1 that is a publication distributed or that had become available to the public through electric communication lines prior to the filing date of the present application, and thus the Appellant should not be granted a patent under the provisions of Article 29(2) of the Patent Act.

Note

<List of Cited Documents, etc.>

1. International Publication No. WO2015/170698

No. 3 Judgment by the body

1 Regarding Article 36(6)(ii) of the Patent Act (violation of requirements for clarity)

(1) The descriptions of the specification, the scope of claims and the drawings of the present application, which were amended by the written amendment submitted on November 11, 2020 (Hereinafter, this amendment is referred to as "the Amendment".), describe the following matters.

"[Claim 1]

A solar battery comprising:

a photovoltaic power generating layer including a semiconductor junction; and

a UV degradation preventing layer provided directly on the photovoltaic power generating layer, wherein

the UV degradation preventing layer contains impurities including impurities contributing to the semiconductor polarity of the UV degradation preventing layer

distributed in concentration in a layer thickness direction and having a maximum value (C_DMax) of the concentration distribution in an interior of the UV degradation preventing layer, and has a layer thickness (d1+d2) within a range of 2 to 60 nm,
the maximum value (C_DMax) being within the following range:
$1\times10^{19}/cm^3\leq$Maximum value (C_DMax)$\leq4\times10^{20}/cm^3$...Formula (1),
the position (A0) (="depth (Dmax)") of the maximum value (C_DMax) being within the following range:
0<depth (Dmax)≤4 nm...Formula (2), and
has a half value (b1) of the maximum value (C_DMax) at a depth position (A1) from a surface of the UV degradation preventing layer on a light incident side, and
the depth position (A1) is within the following range:
Depth position (A0) of Maximum value (C_DMax)<("Depth position (A1)")≤20 nm... Formula (3).

[Claim 2]
A photoelectric converter comprising:
a photoelectron generating layer including a semiconductor junction; and
a UV degradation preventing layer provided directly on the photoelectron generating layer, wherein
the UV degradation preventing layer contains impurities including impurities contributing to the semiconductor polarity of the UV degradation preventing layer distributed in concentration in a layer thickness direction and having a maximum value (C_DMax) of the concentration distribution in an interior of the UV degradation preventing layer, and has a layer thickness (d1+d2) within a range of 2 to 60 nm,
the maximum value (C_DMax) being within the following range:
$1\times10^{19}/cm^3\leq$Maximum value (C_DMax)$\leq4\times10^{20}/cm^3$...Formula (1),
the position (A0) (="depth (Dmax)") of the maximum value (C_DMax) being within the following range:
0<depth (Dmax)≤4 nm...Formula (2), and
has a half value (b1) of the maximum value (C_DMax) at a depth position (A1) from a surface of the UV degradation preventing layer on a light incident side, and
the depth position (A1) is within the following range:
Depth position (A0) of Maximum value (C_DMax)<("Depth position (A1)")≤20 nm... Formula (3)".

"[0004]

...

For the purpose of suppressing such deterioration caused by UV light, there is a technique of coating and sealing a solar battery cell with a sealing material containing a weather-proof agent such as an ultraviolet absorber, a light stabilizer, and the like.

However, this technique deviates from the view of increasing power generation efficiency by effectively utilizing UV light, and causes an increase in the number of manufacturing processes and the cost of the solar battery cell.

..."

"[0009]

...

The photovoltaic power generating layer 102 is configured by a layer region (1) 103 and a layer region (2) 104 configured by semiconductors.

..."

"[0011]

With the maximum value (C_DMax) set within the range of Formula (1), even when a fixed charge or interface state is generated by the irradiation of UV light in an oxide film (natural oxide film) formed on a silicon layer surface of the solar battery interior or on the interface between the oxide film and the silicon layer, carriers or impurity ions in the layer region (4) 111 can combine electric lines of force with the fixed charge, and thus do not substantially change in the internal electric field, and can make the interface state inactive so as not to serve as a recombination center. When the maximum value (C_DMax) deviates from the range of Formula (1), the effect described above becomes difficult to effectively obtained, which is not preferred".

"[0025]

FIG. 1G shows yet another preferred example.

The curve of the effective semiconductor impurity distribution concentration (C_D) of a solar battery 100G shown in FIG. 1G differs from the curve of the effective semiconductor impurity distribution concentration (C_D) in the case of FIG. 1F in terms of the following.

That is, the curve of the effective semiconductor impurity distribution concentration (C_D) of the solar battery shown in FIG. 1G, unlike the case of FIG. 1F, has only one inflection point or substantially only one inflection point.

At a boundary between the layer region (2) 104 and the UV degradation

preventing layer 109, the curve of the effective semiconductor impurity distribution concentration (C_D) changes continuously. Then, the semiconductor polarity of the layer region (2) 104 and the UV degradation preventing layer 109 are the same. That is, the solar battery shown in FIG. 1G has a layer structure of the semiconductor polarities of n/p/p or p/n/n from the side opposite to the incident side of the sunlight.

[0026]

FIG. 1H shows yet another preferred example.

The curve of the effective semiconductor impurity distribution concentration (C_D) of a solar battery 100H shown in FIG. 1H is substantially the same as in FIG. 1G except that the curve has the maximum peak Pmax (3) and the minimum peak Pmin (3) in the portion of the UV degradation preventing layer 109, as in the case of FIG. 1E.

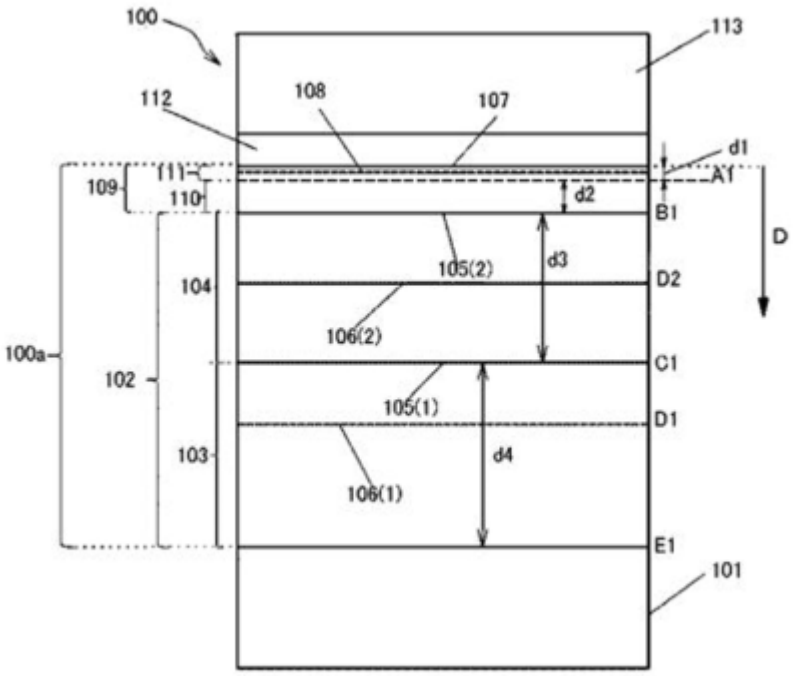
[0027]

FIG. 1I shows yet another preferred example.

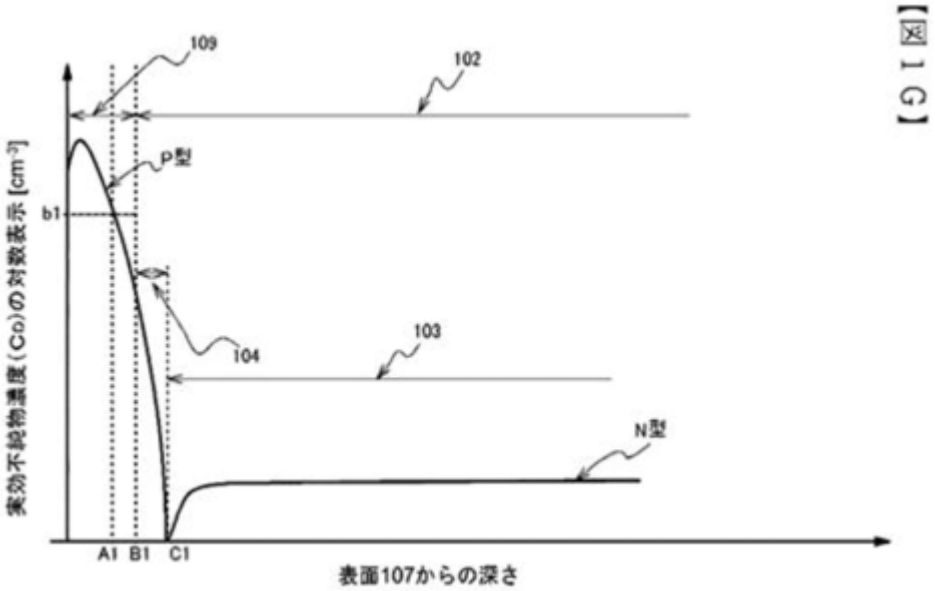
The curve of the effective semiconductor impurity distribution concentration (C_D) of a solar battery 100I shown in FIG. 1I is substantially the same as in FIG. 1G except that the curve has the maximum peak Pmax (3) and the minimum peak Pmin (3) in the portion of the UV degradation preventing layer 109, as in the case of FIG. 1D"

FIG. 1A, FIG. 1G, FIG. 1H, and FIG. 1I are as follows.

【図１Ａ】



【図１Ａ】 [FIG. 1A]



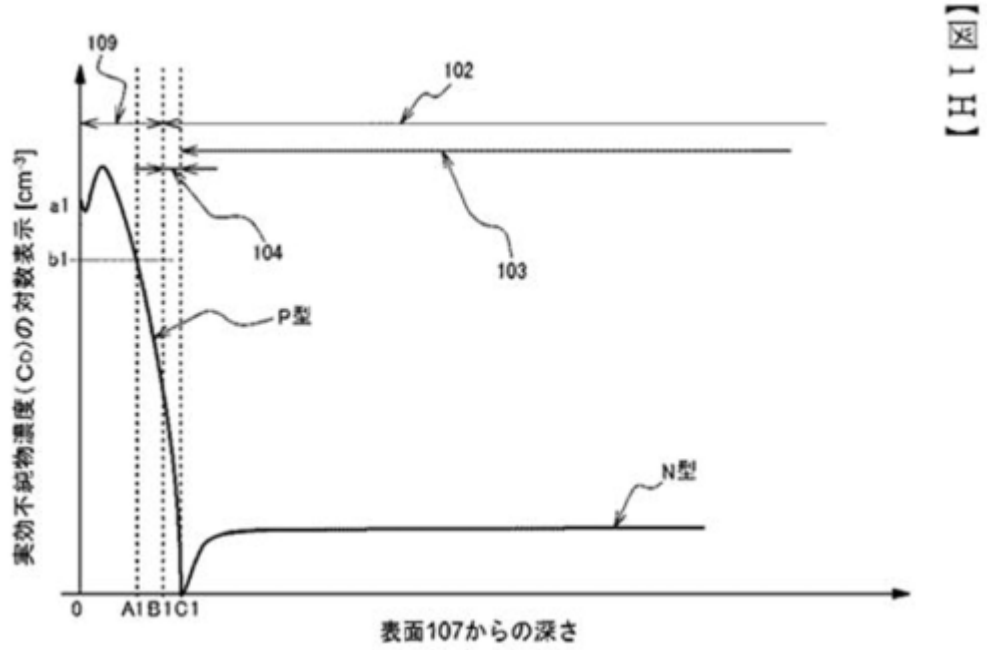
【図１Ｇ】　　[FIG. 1G]

実効不純物濃度（C_D）の対数表示[cm^{-3}]　Logarithmic expression of the effective semiconductor impurity distribution concentration (C_D) [cm^{-3}]

表面１０７からの深さ　Depth from the surface 107

Ｐ型　P-type

Ｎ型　N-type



【図１Ｈ】　　[FIG. 1H]

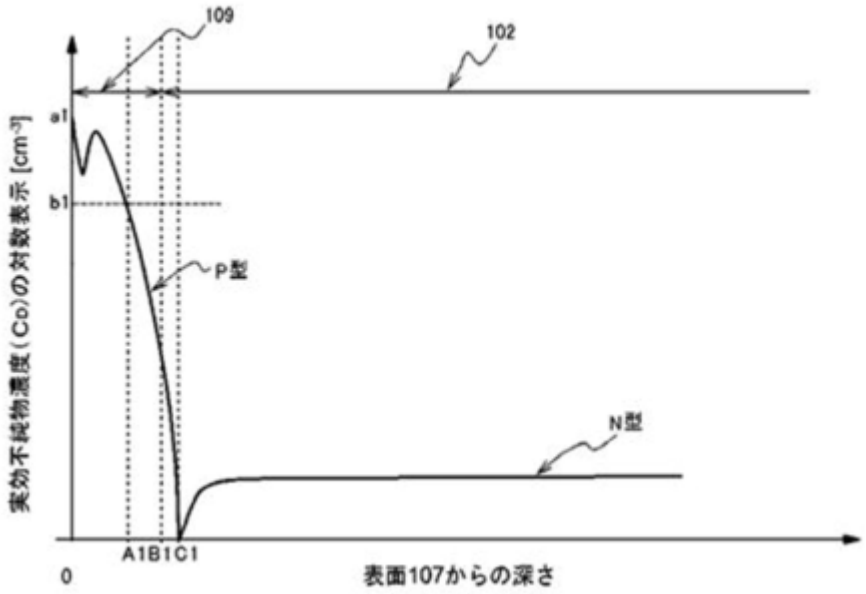
実効不純物濃度（C_D）の対数表示[cm^{-3}]　Logarithmic expression of the

effective semiconductor impurity distribution concentration (C_D) [cm^{-3}]

表面１０７からの深さ　　Depth from the surface 107

Ｐ型　　P-type

Ｎ型　　N-type



【図１１】

【図１Ｉ】　　[FIG. 1I]

実効不純物濃度（C_D）の対数表示[cm^{-3}]　Logarithmic expression of the effective semiconductor impurity distribution concentration (C_D) [cm^{-3}]

表面１０７からの深さ　　Depth from the surface 107

Ｐ型　　P-type

Ｎ型　　N-type

(2) Judgment

A　Regarding the boundary (hereinafter, referred to as "the Boundary of the case") of the "UV degradation preventing layer" and the "photovoltaic power generating layer" (located immediately below it)

(A) Concerning the Boundary of the case, according to the description of the specification of the present application, the following can be said.

a　Since in the section of [FIG. 1G] of [0008], it is described that "FIG. 1G is a graph showing one of the preferred examples of the effective semiconductor impurity distribution concentration (C_D) contained in the photovoltaic power generating part of the solar battery illustrated in FIG. 1A," and in [0025], it is described that "FIG. 1G

shows yet another preferred example," it can be said that an example according to FIG. 1G (hereinafter, referred to as "FIG. 1G Embodiment") is included in Claims 1 and 2. However, the Boundary of the case of FIG. 1G Embodiment is not clear.

That is, according to the description of [0009] that "The photovoltaic power generating part 100a includes a photovoltaic power generating layer 102 and an ultraviolet ray (UV) degradation preventing layer 109. The photovoltaic power generating layer 102 is configured by a layer region (1) 103 and a layer region (2) 104 configured by semiconductors," and according to the description of [0025], in FIG. 1G Embodiment, it can be said that the "UV degradation preventing layer 109" corresponds to the "UV degradation preventing layer" of each claim, and similarly, the "layer region (1) 103" and the "layer region (2) 104" correspond to the "photovoltaic power generating layer" (among them, a "layer region (2) 104" corresponds to "'photovoltaic power generating layer' (immediately below it),") and it can be understood that the Boundary of the case of FIG. 1G Embodiment is made to be a boundary of the "UV degradation preventing layer 109" and the "layer region (2) 104".

However, according to FIG. 1G and the description of [0025] that "the semiconductor polarity of the layer region (2) 104 and the UV degradation preventing layer 109 are the same," since it can be understood that the "UV degradation preventing layer 109" and the "layer region (2) 104" are both P-type and the polarity of them are the same, the location of the Boundary of the case between these layers cannot be determined from the viewpoint of polarity.

Furthermore, in [0025], concerning FIG. 1G Embodiment, it is described that "At a boundary between the layer region (2) 104 and the UV degradation preventing layer 109, the curve of the effective semiconductor impurity distribution concentration (C_D) changes continuously," and when viewed from FIG. 1G, the curve of the effective semiconductor impurity distribution concentration just smoothly and monotonously decreases without an inflection point or maximum or minimum near the Boundary of the case. So, the location of the Boundary of the case cannot be determined from the viewpoint of impurity distribution concentration.

Furthermore, since it can be understood that the materials forming the "UV degradation preventing layer 109" and the "layer region (2) 104" are both silicon (Si) (see [0028]), the location of the Boundary of the case cannot be determined from the viewpoint of material.

In addition, since the Boundary of the case is a boundary of the "UV degradation preventing layer" and the "photovoltaic power generating layer," although it can be said that a function of "UV degradation preventing" and a function of "photovoltaic power

generating" are different, as described above, these layers cannot be distinguished from any viewpoint of polarity, impurity distribution concentration, and material, and even by looking at the description in the specification of the present application, no clue can be found to determine the Boundary of the case quantitatively.

And, even by looking at other descriptions in the specification of the present application, it is unclear how to determine the Boundary of the case in FIG. 1G Embodiment.

Therefore, the Boundary of the case of FIG. 1G Embodiment is not clear.

b According to the descriptions of [0009] and [0026], in an example according to FIG. 1H (hereinafter, referred to as "FIG. 1H Embodiment"), it can be said that the "UV degradation preventing layer 109" corresponds to the "UV degradation preventing layer" of each claim, and similarly, the "layer region (1) 103" and the "layer region (2) 104" correspond to a "photovoltaic power generating layer" (among them, a "layer region (2) 104" corresponds to 'photovoltaic power generating layer' (immediately below it),") and it can be understood that the Boundary of the case of FIG. 1H Embodiment is made to be a boundary of the "UV degradation preventing layer 109" and the "layer region (2) 104".

Further, according to the descriptions of [0009] and [0027], in an example according of FIG. 1I (hereinafter, referred to as "FIG. 1I Embodiment"), it can be said that the "UV degradation preventing layer 109" corresponds to the "UV degradation preventing layer" of each claim, and similarly, the "photovoltaic power generating layer 102" corresponds to the "photovoltaic power generating layer" of each claim, and it can be understood that the Boundary of the case of FIG. 1I Embodiment is made to be a boundary of the "UV degradation preventing layer 109" and the "photovoltaic power generating layer 102".

Therefore, the Boundaries of the case of FIG. 1H Embodiment and FIG. 1I Embodiment are also not clear, for the same reason as in FIG. 1G Embodiment.

c In this way, the Boundary of the case is not clear in FIG. 1G Embodiment, FIG. 1H Embodiment, and FIG. 1I Embodiment, which are obviously included in each claim.

(B) As described in (A) above, wherebythe Boundary of the case is not clear in FIG. 1G Embodiment, FIG. 1H Embodiment, and FIG. 1I Embodiment, which are obviously included in each claim, it cannot be said that the Boundary of the case immediately becomes clear from the terms of the "UV degradation preventing layer" and the

"photovoltaic power generating layer" of each claim, and this understanding is not affected by the other specified matters of each claim.

Then, it should be said that the Boundary of the case in each claim is also not clear.

B Regarding "a layer thickness (d1+d2) within a range of 2 to 60 nm" of Claims 1 and 2

As examined in A above, it is unclear how the boundary of the "UV degradation preventing layer" and the "photovoltaic power generating layer" (immediately below it) is determined.

When the boundary of the "UV degradation preventing layer" and the "photovoltaic power generating layer" (immediately below it) is not determined, the layer thickness of the UV degradation preventing layer becomes unclear.

Accordingly, since the layer thickness of the UV degradation preventing layer is unclear, the Claims 1 and 2 are not clear whether or not having the layer thickness (d1+d2) of the UV degradation preventing layer within a range of 2 to 60 nm.

(3) Regarding the Appellant's allegation

The Appellant, in the written opinion submitted on November 11, 2020, alleges that " the boundary is defined with an inflection point of impurity distribution concentration, even in case of same polarity ".

However, as examined in (2) above, the inventions described in Claims 1 and 2 of the present application involve those having no inflection point in boundary region of the photovoltaic power generating layer and the UV degradation preventing layer (see FIG. 1G, FIG. 1H, and FIG. 1I above).

Therefore, the Appellant's allegation is not based on the descriptions of the specification and drawings of the present application.

As described above, the Appellant's allegation cannot be accepted.

(4) Summary

Therefore, the inventions according to Claims 1 and 2 of the present application are not clear.

2 Regarding Article 36(6)(i) of the Patent Act (violation of requirements for support)

(1) It is recognized that the problems to be solved of the inventions described in Claims

1 and 2 of the present application (hereinafter, referred to as "the Problems of the case") are that the conventional art for suppressing deterioration by UV light in which the power generation efficiency of the solar cell decreases with the irradiation history of UV light, causes an increase in the number of manufacturing processes and costs ([0004]).

And, it is recognized that so as to solve the Problems of the case, the inventions described in Claims 1 and 2 provide the "UV degradation preventing layer" as described in Claims 1 and 2 as means for solving the problems thereof.

So, it will be examined whether or not it can be recognized bya person skilled in the art that the Problems of the case can be solved by the "UV degradation preventing layer" specified in Claims 1 and 2, in light of the description of the specification and the like of the present application and common general technical knowledge.

(2) According to the description of [0011] of the specification of the present application, it is recognized that a principle for solving the problems of the case (hereinafter, referred to as "the Principle solving the problems of the case") is that electric lines of force generated by the fixed charge existing in an oxide film (natural oxide film) formed on a silicon layer surface of the solar battery interior or on the interface between the oxide film and the silicon layer (hereinafter, the inside of the oxide film and the interface are collectively referred to as "the Place of the case") are combined by carriers or impurity ions in the UV deterioration preventing layer, thereby substantially not changing in the internal electric field, and making the interface state inactive so as not to serve as a recombination center.

Based on the Principle solving the problems of the case, in order to solve the problem, although it is considered that the polarity of the fixed charge existing at the Place of the case is important, it is not specified in Claims 1 and 2 whether the fixed charge is a positive charge, a negative charge, or both a positive charge and a negative charge. Then, it will be examined whether or not it can be recognized that the inventions described in Claims 1 and 2 can solve the Problems of the case, regardless of the polarity of the fixed charge.

First, looking at the aspect in which both positive charge and a negative charge exist at the same time (distributed) as fixed charges in the Place of the case, since an internal electric field or electric lines of force remain in the Place of the case, it is considered that the "UV degradation preventing layer" is unnecessary in the first place. Therefore, such an aspect has nothing to do with solving the Problems of the case, and therefore, it can be said that it is not recognized that the problems can be solved by each

of the inventions.

Next, looking at the aspect in which only a positive charge or a negative charge exists as a fixed charge in the Place of the case, from the viewpoint of combining the electric lines of force, it is considered that the "UV degradation preventing layer" requires a semiconductor having a polarity that produces a small number of carriers having a polarity opposite to the polarity of the fixed charge. However, Claims 1 and 2 do not specify the polarity of the semiconductor used for the "UV degradation preventing layer". Therefore, since the inventions described in Claims 1 and 2 include the aspect recognized as unable to solve the Problems of the case, it can be said that it is not recognized that each of the inventions can solve the Problem of the case.

In this way, according to the Principle solving the problems of the case which is understood from the description of the specification of the present application, it cannot be said that it is recognized that the inventions described in Claims 1 and 2 can solve the Problems of the case, regardless of the polarity of the fixed charge existing in the Place of the case. That is, it cannot be said that the inventions described in Claims 1 and 2 in which the polarity of the fixed charge in the Place of the case is not specified can solve the Problems of the case, in light of the Principle solving the problems of the case.

(3) Then, looking at an embodiment described in the specification and the like of the present application, [0031] to [0034] describe a p+pn type element structure, and it is understood that a "p+" layer corresponds to the "UV degradation preventing layer," and a "p" layer and an "n" layer correspond to the "photovoltaic power generating layer," respectively.

If such a "UV degradation preventing layer" is a p-type such as a "p+" layer, since a small number of carriers generated in the layer are electrons, according to the Principle solving the problems of the case, it is understood that the polarity of the fixed charge generated at the Place of the case must be positive, in order to solve the Problems of the case. Therefore, in order for the description of each claim to meet the requirements for support, in the embodiment of the p+pn type element structure, it should be said that not only the example in which the polarity of the fixed charge is positive, but also the example in which the polarity of the fixed charge is negative needs to be presented. Also, there is no description about the polarity of the fixed charge in the embodiment described in the specification and the like of the present application. Then, there is no other description of embodiments in the specification and the like of the present application.

Therefore, even considering the embodiment described in the specification and

the like of the present application, it cannot be said that it is recognized that the inventions described in Claims 1 and 2 in which the polarity of the fixed charge in the Place of the case is not specified can solve the Problems of the case.

(4) According to the above, since it cannot be said that it is recognized that the inventions described in Claims 1 and 2 in which the fixed charge in the Place of the case is not specified can solve the Problems of the case, the inventions described in Claims 1 and 2 are not described in the detailed description of the invention.

(5) Regarding the Appellant's allegation

The Appellant, in the written opinion submitted on November 11, 2020, alleges that "When charged by UV light, potential modulation may occur on the incident surface of the semiconductor substrate. For example, in a P+NP type solar battery, when positive charge is generated by UV light, the light charge generated by sunlight easily moves to the incident surface side of the semiconductor substrate without moving to the N type layer. On the incident surface, there is an interface between the semiconductor and the insulator, where the interface state exists. The interface state increases the recombination rate of the light charge, makes the generated light charge undetectable, and reduces the sensitivity. Originally, in the case of a P+NP type, only positive charge causes deterioration of sensitivity, and in the case of an N+PN type, only negative charge causes deterioration of sensitivity. However, from the experimental results, the polarity of the fixed charge generated by UV light can be positive or negative, and also, depending on the UV light irradiation time, the total charge may be high in positive charge or high in negative charge. Therefore, it is necessary to prevent deterioration regardless of which polarity is charged. The solution to this is the relationship specified in Claims 1 and 2 after amendment".

Although there are unclear parts in the Appellant's allegation, the outline can be understood that although the polarity of the fixed charge generated at the Place of the case may be positive or negative, and the charge caused by the fixed charge at the Place of the case may be positive or negative, when the conditions specified in each claim are satisfied, the Problems of the case can be solved regardless of the polarity of charging at the place of the case.

However, there is no description at all in the specification and the like of the present application, and furthermore, according to the description of [0011], it is obvious that the polarity of the fixed charge at the Place of the case is important for

solving the Problems of the case. Therefore, the Appellant's allegation is not based on the description of the specification and the like of the present application, and thus cannot be accepted.

(6) Summary

Therefore, the inventions described in Claims 1 and 2 of the present application are not described in the detailed description of the invention.

3 Regarding Article 29(2) of the Patent Act (inventive step)

(1) Recognition of the Invention

Although in Claim 2 of the present application, as described in 1 above, there is a deficiency due to lack of clarity in how to determine the boundary between the "UV degradation preventing layer" and the "photoelectron layer" (immediately below it), since it is described in [0021] of the specification and the like of the present application that "In the example of FIG. 1B, when the layer region 103 is the n-type, for example, the layer region 104 is the p-type and the layer region 109 is the n-type. In the case of the present invention, it is easily conceivable that the layer regions may have a polarity in which n-type and the p-type are switched, which is the category of the present invention," and it is described in [0009] of the specification and the like of the present application that "The photovoltaic power generating layer 102 is configured by a layer region (1) 103 and a layer region (2) 104 configured by semiconductors" and that "The UV degradation preventing layer 109 is configured by a layer region (3) 110 and a layer region (4) 111, contains semiconductor impurities, and is imparted with a predetermined semiconductor polarity," it is understood that Claim 2 includes at least the aspect in which the boundary between the "UV degradation preventing layer" and the "photoelectron generating layer" (immediately below it) is determined because the polarities of the two layers are different.

Then, hereinafter, interpreting that Claim 2 of the present application includes at least such an aspect, the invention according to Claim 2 of the present application (hereinafter, referred to as "the Invention") is recognized as described in Claim 2.

It is described again as follows.

"[Claim 2]

A photoelectric converter comprising:

a photoelectron generating layer including a semiconductor junction; and

a UV degradation preventing layer provided directly on the photoelectron generating layer, wherein

the UV degradation preventing layer contains impurities including impurities contributing to the semiconductor polarity of the UV degradation preventing layer distributed in concentration in a layer thickness direction and having a maximum value (C_DMax) of the concentration distribution in an interior of the UV degradation preventing layer, and has a layer thickness (d1+d2) within a range of 2 to 60 nm,
the maximum value (C_DMax) being within the following range:
$1\times10^{19}/cm^3 \leq$ Maximum value (C_DMax) $\leq 4\times10^{20}/cm^3$...Formula (1),
the position (A0) (="depth (Dmax)") of the maximum value (C_DMax) being within the following range:
0<depth (Dmax)≤4 nm...Formula (2), and
has a half value (b1) of the maximum value (C_DMax) at a depth position (A1) from a surface of the UV degradation preventing layer on a light incident side, and
the depth position (A1) is within the following range:
Depth position (A0) of Maximum value (C_DMax)<("Depth position (A1)")≤20 nm... Formula (3)".

(2) Regarding Cited Document

In International Publication No. WO2015/170698 (hereinafter, referred to as Cited Document 1) cited in the reasons for refusal by the body, the following matters are described (the underlines are applied by the body; the same applies hereinafter).
A "[0012] The present invention is the result of close investigation and research into such points, and it is therefore a main object of the present invention to provide a solid-state light-receiving device for ultraviolet light that is simple in structure and at least substantially free of sensitivity deterioration and decreases in dark current characteristics, even if continually irradiated by ultraviolet rays of a wide ultraviolet region of 10 to 400 nm for a long period of time.

It is also another object of the present invention to provide a solid-state light-receiving device for ultraviolet light that is simple in structure, capable of accurately and appropriately measuring an amount of irradiation of ultraviolet light harmful to the human body, capable of easy integration with a sensor of a peripheral circuit, and stable in terms of initial characteristics, even in response to long-term irradiation of ultraviolet rays in a wide ultraviolet wavelength region".

"[0023] FIG. 1 is an example of a schematic explanatory view for explaining a suitable example of a configuration of a solid-state light-receiving device for ultraviolet light according to the present invention.

A main portion 100 of the solid-state light-receiving device for ultraviolet light illustrated in FIG. 1 comprises a photodiode (PD) 100a inside a semiconductor substrate 101 containing silicon (Si) as a main component.

The photodiode (PD) 100a is composed of layer regions 102a, 110a, and 111a.

The layer region 102a is composed of a semiconductor layer region 103a of a first conductive type, and a semiconductor layer region 104a embedded in an upper portion of the semiconductor layer region 103a.

Upper portion surfaces of the semiconductor layer region 103a and the semiconductor layer region 104a are aligned as illustrated.

The semiconductor layer region 104a is a second conductive type that differs in polarity from the first conductive type. That is, given that the first conductive type is P, for example, the second conductive type is N.

A semiconductor junction 105a (1) is formed by the semiconductor layer region 103a and the semiconductor layer region 104a.

A semiconductor layer region 109a having the same polarity as the semiconductor layer region 103a is provided on the semiconductor layer region 104a.

A semiconductor junction 105a (2) is formed by the semiconductor layer region 103a and the semiconductor layer region 109a.

The semiconductor layer region 103a and the semiconductor layer region 109a contain first semiconductor impurities (1) and are therefore first conductive types. It should be noted that 'semiconductor impurities' are also written as 'impurity atoms' hereinafter.

[0024] Next, a description will be given with reference to Fig. 1A as well as FIG. 1B.

The semiconductor impurities (1) in the semiconductor layer region 103a are contained in the semiconductor layer region 103a in a state distributed in a layer thickness direction of the semiconductor layer region 103a.

A maximum content concentration position (D1) 106a of the semiconductor impurities (1) is provided in a position downward from the semiconductor junction 105a (1) in the distribution of the semiconductor impurities (1) in the layer thickness direction of the semiconductor layer region 103a. It should be noted that 'maximum content concentration position' is also written as 'maximum concentration position' hereinafter.

For the semiconductor layer region 109a similar to the semiconductor layer region 103a, the semiconductor impurities (1) are contained in the semiconductor layer region 109a in a state distributed in the layer thickness direction, and a maximum

content concentration position 108a of the semiconductor impurities (1) is provided.

[0025] The semiconductor layer region 109a includes the maximum concentration position 108a in an upward portion thereof, and comprises the layer region 111a having a thickness d1 (the thickness from a position of a surface 107 of the semiconductor substrate to a position A1 in a depth direction) regarded as free or effectively free of absorption of UV-A and UV-B light.

[0026] In the present invention, the position A1 does not hinder design, even if at the same position as the maximum concentration position 108a. Nevertheless, if the thickness d1 regarded as free or effectively free of absorption of UV-A and UV-B light is to be maintained, the position A1 is preferably below the maximum concentration position 108a in terms of manufacturing allowance.

[0027] The layer thickness of the layer region 110a between the position A1 and a position B1 may be determined in accordance with a preferred design as appropriate under the condition that the maximum concentration position 108a can be provided in a suitable position.

The inventors of the present application created a solid-state light-receiving device for ultraviolet light comprising the main portion 100 having the configuration described above, and repeatedly conducted earnest research and investigations while changing a content and content distribution of the semiconductor impurities contained in the semiconductor layer regions 103a, 104a, and 109a in a great variety of ways, thereby discovering a solid-state light-receiving device for ultraviolet light free or substantially free of sensitivity and dark current deterioration even with long-term continuous irradiation of far ultraviolet light and vacuum ultraviolet light.

According to the results of the research and investigations of the inventors of the present application, the solid-state light-receiving device for ultraviolet light was confirmed to be free or substantially free of sensitivity deterioration and increases in dark current as long as the concentration of impurity atoms at the maximum concentration position 108a is 1×10^{19} cm^{-3} or greater.

Results clearly showed that, with this concentration, it is possible to terminate all or substantially all lines of electric force produced by a fixed charge that occurs by irradiation of far ultraviolet light and vacuum ultraviolet light and, as a result, obtain a solid-state light-receiving device for ultraviolet light that is free or substantially free of sensitivity and dark current deterioration even with long-term continuous irradiation of far ultraviolet light and vacuum ultraviolet light.

According to the results of the research and investigations of the inventors of the present application, it is clear that the characteristics described above can be further

strengthened by providing the maximum concentration position 108a described above in a range of depth of within a few nm from the surface 107 of the semiconductor substrate 101.

The present invention is based on these points.

The position of the semiconductor junction 108a is preferably formed at about 50 nm to 80 nm, for example, to increase sensitivity to ultraviolet light.

However, to decrease an electric field strength of the semiconductor junction 108a to the extent possible and decrease the dark current that occurs at the semiconductor junction, the concentration of the semiconductor impurities of the semiconductor layer region 109a near the semiconductor junction 105a (2) is preferably decreased. To avoid complexities in manufacture, the concentration of the semiconductor impurities of the semiconductor layer region 109a near the semiconductor junction 105a (2) is preferably set to 1×10^{17} cm^{-3} or less and 1×10^{15} cm^{-3} or greater. Preferably, the concentration is set to about 1×10^{16} cm^{-3}.

The light-receiving device according to the present invention configured as described above and a conventional light-receiving device were subjected to continual irradiation for 1,500 minutes using a deuterium lamp having a light intensity of 120 $\mu W/cm^2$ at a light wavelength of 204 nm as a light source, and the following was confirmed.

That is, with the light-receiving device according to the present invention, neither a decrease in light sensitivity nor a decrease in dark current characteristics occurred. In contrast, with the light-receiving device set forth in Patent Document 1, the light sensitivity of the ultraviolet bandwidth (wavelength: 200 to 380 nm) deteriorated by at least 50%, and the dark current increased at least ten fold with respect to the initial value.

In the case of the present invention, it was confirmed that, even if the irradiation time were extended to 12,000 minutes, a deterioration in light sensitivity and an increase in dark current were both within a few percent and unproblematic for all practical purposes.

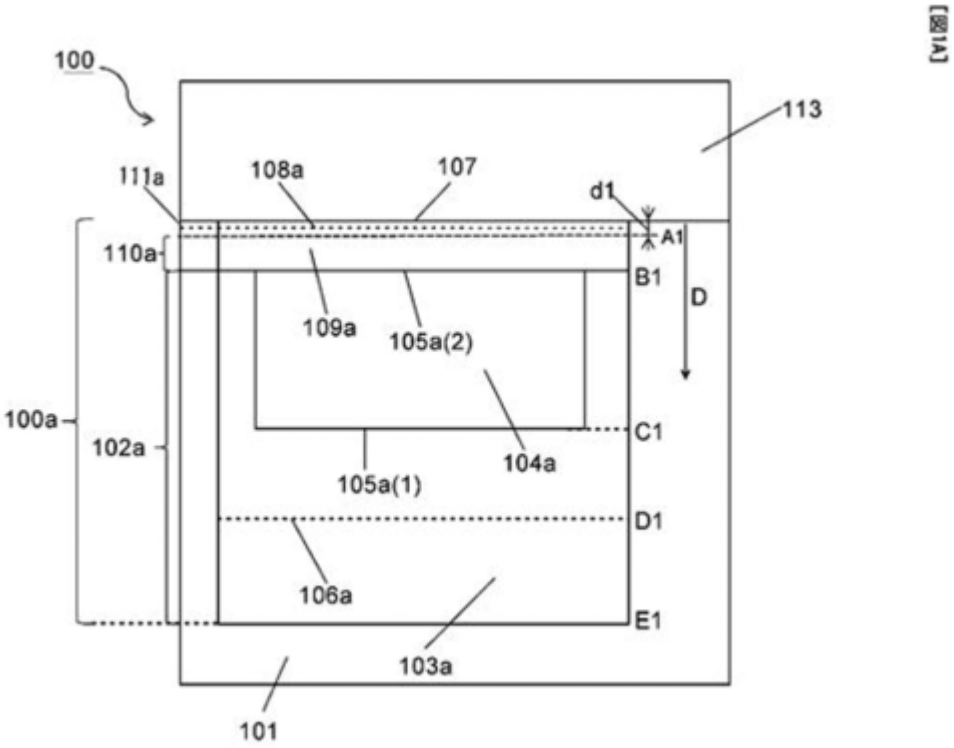
The solid-state light-receiving device for ultraviolet light according to the present invention, even if manufactured as a product that does not receive irradiation of far ultraviolet light or vacuum ultraviolet light, is free of deterioration of sensitivity and dark current characteristics even if irradiated by far ultraviolet light or vacuum ultraviolet light by an irresistible force, and thus, in terms of application, is not limited to a product that measures an amount of irradiated far ultraviolet light and vacuum ultraviolet light".

"[0055] The layer thickness of the layer region 110b between the position A1 and the position B1 may be determined in accordance with a preferred design as appropriate under the condition that the maximum concentration position (2-2) 108b can be provided in a suitable position. In a suitable embodiment of the present invention, the position A1 and the position A2, and the position B1 and a position B2 are preferably the same or substantially the same, respectively.

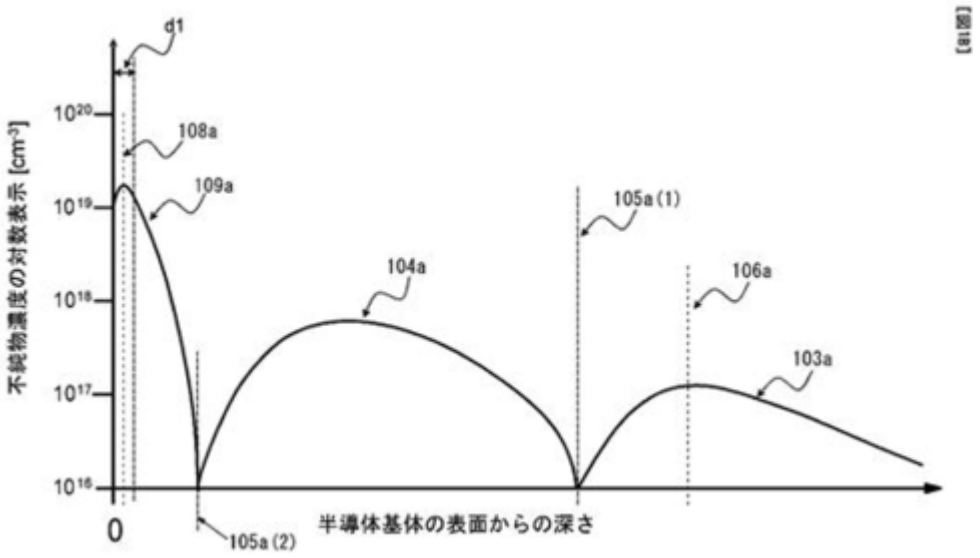
[0056] The layer thickness of the layer region 110a and the layer thickness of the layer region 110b are preferably determined as appropriate in accordance with design preferences so as to satisfy the conditions described above. Specifically, the layer thickness of the layer region 110a and the layer thickness of the layer region 110b are preferably 6 nm or less, and more preferably 2 nm or less".

FIG. 1A and FIG. 1B are as follows.

Further, according to the description of FIG. 1A, it can be seen that the layer region 110a is configured by the semiconductor layer region 109a between the position A1 and the position B1.



【図１Ａ】 [FIG. 1A]



【図１Ｂ】 [FIG. 1B]

不純物濃度の対数表示[㎝$^{-3}$] Logarithmic expression of impurity concentration [cm^{-3}]

半導体基体の表面からの深さ Depth from the surface of the semiconductor substrate

B Cited Invention

Therefore, Cited Document 1 describes the following invention (hereinafter, referred to as "the Cited Invention").

"A solid-state light-receiving device for ultraviolet light ([0023]) comprising a photodiode (PD) 100a composed of layer regions 102a, 110a, and 111a inside a semiconductor substrate 101 containing silicon (Si) as a main component, ([0023]) wherein

the layer region 102a is composed of a semiconductor layer region 103a of a first conductive type, and a semiconductor layer region 104a embedded in an upper portion of the semiconductor layer region 103a, ([0023])

a semiconductor junction 105a (1) is formed by the semiconductor layer region 103a and the semiconductor layer region 104a, ([0023])

a semiconductor layer region 109a having the same polarity as the semiconductor layer region 103a is provided on the semiconductor layer region 104a, ([0023])

the layer region 110a is configured by the semiconductor layer region 109a between a position A1 and a position B1, (FIG. 1A)

a semiconductor junction 105a (2) is formed by the semiconductor layer region

103a and the semiconductor layer region 109a, ([0023])

the semiconductor layer region 109a includes the maximum concentration position 108a in an upward portion thereof, and comprises the layer region 111a having a thickness d1 (the thickness from a position of a surface 107 of the semiconductor substrate to a position A1 in a depth direction) regarded as free or effectively free of absorption of UV-A and UV-B light, ([0025])

the concentration of impurity atoms at the maximum concentration position 108a is 1×10^{19} cm^{-3} or greater, and with this concentration, it is possible to obtain a solid-state light-receiving device for ultraviolet light that is free or substantially free of sensitivity and dark current deterioration even with long-term continuous irradiation of far ultraviolet light and vacuum ultraviolet light, ([0027])

the maximum concentration position 108a is provided in a range of depth of within a few nm from the surface 107 of the semiconductor substrate 101, ([0027]) and

to decrease an electric field strength of the semiconductor junction 108a to the extent possible and decrease the dark current that occurs at the semiconductor junction, the concentration of the semiconductor impurities of the semiconductor layer region 109a near the semiconductor junction 105a (2) is decreased. ([0027])"

(3) Comparison

The Invention and the Cited Invention are compared.

A The Cited Invention is "a solid-state light-receiving device for ultraviolet light," and composed of " 'a layer region 102a' forming 'a semiconductor junction 105a (1) by the semiconductor layer region 103a and the semiconductor layer region 104a'," so that it is natural to think that an electric charge is generated in the layer region 102a when irradiated with ultraviolet rays.

Accordingly, " 'a layer region 102a' 'composed of a semiconductor layer region 103a of a first conductive type, and a semiconductor layer region 104a embedded in an upper portion of the semiconductor layer region 103a' and forming 'a semiconductor junction 105a (1) ' ' by the semiconductor layer region 103a and the semiconductor layer region 104a' " of the Cited Invention corresponds to "a photoelectron generating layer including a semiconductor junction" of the Invention, and

"a solid-state light-receiving device for ultraviolet light" of the Cited Invention corresponds to "a photoelectric converter" of the Invention.

B The Cited Invention is specified as "the layer region 110a is configured by the semiconductor layer region 109a between a position A1 and a position B1," "the

semiconductor layer region 109a includes the maximum concentration position 108a in an upward portion thereof, and comprises the layer region 111a having a thickness d1 (the thickness from a position of a surface 107 of the semiconductor substrate to a position A1 in a depth direction) regarded as free or effectively free of absorption of UV-A and UV-B light," and "the concentration of impurity atoms at the maximum concentration position 108a is 1×10^{19} cm^{-3} or greater, and with this concentration, it is possible to obtain a solid-state light-receiving device for ultraviolet light that is free or substantially free of sensitivity and dark current deterioration even with long-term continuous irradiation of far ultraviolet light and vacuum ultraviolet light". Furthermore, the semiconductor layer region 109a is a first conductive type and the semiconductor layer region 104a is a second conductive type, and the polarities of the two layers are different, so that it can be said that the layer region 110a and the layer region 111a configured by the semiconductor layer region 109a are layers for preventing the UV deterioration of the solid-state light-receiving device for ultraviolet light.

Further, "impurity atoms" of the Cited Invention correspond to "impurities contributing to the semiconductor polarity" of the Invention.

Then, " 'the layer region 110a is configured by the semiconductor layer region 109a between a position A1 and a position B1,' 'a semiconductor layer region 109a having the same polarity as the semiconductor layer region 103a is provided on the semiconductor layer region 104a' of 'a layer region 102a,' and 'the semiconductor layer region 109a includes the maximum concentration position 108a in an upward portion thereof, and comprises the layer region 111a having a thickness d1 (the thickness from a position of a surface 107 of the semiconductor substrate to a position A1 in a depth direction) regarded as free or effectively free of absorption of UV-A and UV-B light', and 'the concentration of impurity atoms at the maximum concentration position 108a is 1×10^{19} cm^{-3} or greater, and with this concentration, it is possible to obtain a solid-state light-receiving device for ultraviolet light that is free or substantially free of sensitivity and dark current deterioration even with long-term continuous irradiation of far ultraviolet light and vacuum ultraviolet light' " of the Cited Invention corresponds to "comprising 'a UV degradation preventing layer provided directly on the photoelectron generating layer, wherein the UV degradation preventing layer contains impurities including impurities contributing to the semiconductor polarity of the UV degradation preventing layer distributed in concentration in a layer thickness direction and having a maximum value (C_DMax) of the concentration distribution in an interior of the UV degradation preventing layer', and 'the maximum value (C_DMax) being within the

following range: $1\times10^{19}/cm^3 \leq$ Maximum value (C_DMax) $\leq 4\times10^{20}/cm^3$...Formula (1) '" of the Invention.

C Therefore, the Invention and the Cited Invention are identical and different in the following configurations.

(Corresponding Feature)
"A photoelectric converter comprising:
a photoelectron generating layer including a semiconductor junction; and
a UV degradation preventing layer provided directly on the photoelectron generating layer, wherein
the UV degradation preventing layer contains impurities including impurities contributing to the semiconductor polarity of the UV degradation preventing layer distributed in concentration in a layer thickness direction and having a maximum value (C_DMax) of the concentration distribution in an interior of the UV degradation preventing layer,
the maximum value (C_DMax) being within the following range:
$1\times10^{19}/cm^3 \leq$ Maximum value (C_DMax) $\leq 4\times10^{20}/cm^3$...Formula (1)".

(Different Features)
Concerning the UV degradation preventing layer, in the Invention,
(i) "has a layer thickness (d1+d2) within a range of 2 to 60 nm,"
(ii) "the position (A0) (="depth (Dmax)") of the maximum value (C_DMax) being within the following range:
0<depth (Dmax)≤4 nm...Formula (2),"
(iii) "has a half value (b1) of the maximum value (C_DMax) at a depth position (A1) from a surface of the UV degradation preventing layer on a light incident side, and
the depth position (A1) is within the following range:
Depth position (A0) of Maximum value (C_DMax)<("Depth position (A1)")≤20 nm... Formula (3),"
whereas it is not apparent whether the Cited Invention has similar features.

(4) Judgment
A Regarding Different Features
(A) Regarding (ii), since the Cited Invention is recognized as "the maximum concentration position 108a is provided in a range of depth of within a few nm from the

surface 107 of the semiconductor substrate 101," it is merely a matter that could have been appropriately made by a person skilled in the art to set the maximum concentration position 108a within a depth of 4 nm or less.

(B) Concerning (i), as described in (2) B above, since the "layer region 110a" and the "layer region 111a" of the Cited Invention correspond to the "UV degradation preventing layer" of the Invention, it can be said that the configuration of the Cited Invention corresponding to "a layer thickness (d1+d2)" (of the UV degradation preventing layer) of the Invention is the combined thickness of the "layer region 110a" and "layer region 111a". Concerning the layer thickness of the "layer region 110a", since [0056] of Cited Document 1 describes that "the layer thickness of the layer region 110a and the layer thickness of the layer region 110b are preferably 6 nm or less, and more preferably 2 nm or less," it can be understood that it is "6 nm or less".

Next, concerning the film thickness of the "layer region 111a," since [0025] of Cited Document 1 describes that "comprises the layer region 111a having a thickness d1 (the thickness from a position of a surface 107 of the semiconductor substrate to a position A1 in a depth direction)," [0027] of Cited Document 1 describes that "providing the maximum concentration position 108a" "in a range of depth of within a few nm from the surface 107 of the semiconductor substrate 101," and [0026] of Cited Document 1 describes that "the position A1 does not hinder design, even if at the same position as the maximum concentration position 108a," it can be understood that it may be "within a few nm".

Accordingly, in the Cited Invention, it can be said that the layer thickness combining the layer region 110a and the layer region 111a is assumed to be about a value obtained by adding a value of 6 nm or less and a value of within a few nm depth from the surface 107 of the semiconductor substrate.

Therefore, the point of (i) above is merely a matter that could have been appropriately made by a person skilled in the art.

(C) Concerning (iii), the Cited Invention is recognized as "the semiconductor layer region 109a includes the maximum concentration position 108a in an upward portion thereof," "the concentration of impurity atoms at the maximum concentration position 108a is 1×10^{19} cm^{-3} or greater," "the maximum concentration position 108a is provided in a range of depth of within a few nm from the surface 107 of the semiconductor substrate 101," and "to decrease an electric field strength of the semiconductor junction 108 to the extent possible and decrease the dark current that occurs at the semiconductor

junction, the concentration of the semiconductor impurities of the semiconductor layer region 109a near the semiconductor junction 105a (2) is decreased".

In this way, in the Cited Invention, concerning the concentration of impurity atoms, since the maximum concentration position 108a exists, and the concentration of the semiconductor impurities of the semiconductor layer region 109a near the semiconductor junction 105a (2) is decreased, it is understood that a position of a half value of the maximum concentration of the impurity atoms is not so far from the maximum concentration position 108a (Further, since [0023] of Cited Document 1 describes that " 'semiconductor impurities' are also written as 'impurity atoms' hereinafter." in Cited Document 1, 'semiconductor impurities' and 'impurity atoms' are used in the same meaning.).

Then, for example, from the descriptions of FIG. 1A and FIG. 1B of Cited Document 1, it can be said that the position of the half value of the maximum concentration of the impurity atoms in the Cited Invention is assumed to be about a value obtained by adding a value of 6 nm or less and a value of within a few nm depth from the surface 107 of the semiconductor substrate. That is, from FIG. 1A and FIG. 1B, since it can be seen that the concentration of the impurity atoms in the semiconductor junction 105a (2) between the layer region 111a and the layer region 102a is $1\times10^{16}/cm^{-3}$, and the concentration of the impurity atoms at the maximum concentration position 108a is 1×10^{19} cm^{-3} or greater, the position of the half value of the maximum concentration of the impurity atoms exists in the region combining the layer region 110a and the layer region 111a. Then, as examined in (B) above, since the layer thickness combining the layer region 110a and the layer region 111a is assumed to be about a value obtained by adding a value of 6 nm or less and a value of within a few nm depth from the surface 107 of the semiconductor substrate, in that case, it can be said that the position of the half value of the maximum concentration of the impurity atoms is: Maximum concentration position 108a≤ Position of half value of the maximum concentration≤ adding a value of within a few nm and a value of 6nm or less.

Therefore, in the Cited Invention, it is merely a matter that could have been appropriately made by a person skilled in the art to set the position of the half value of the maximum concentration of the impurity atoms to:
Maximum concentration position 108a≤ Position of half value of the maximum concentration≤20 nm.

B Accordingly, in the Cited Invention, it is merely a matter that could have been

appropriately made by a person skilled in the art to make the configuration of the Invention according to Different Features.

C Then, even when considering Different Features comprehensively, the function and effect exerted by the Invention is merely within a range expected from the function and effect of the Cited Invention, and thus cannot be regarded as a particularly distinguishing effect.

D Regarding the Appellant's allegation

(A) The Appellant, in the written opinion submitted on November 11, 2020, alleges that "Cited Document 1 (International Publication No. WO2015/170698) does not disclose the relationship specified in Claims 1 and 2 after amendment. It should be difficult for even a person skilled in the art considering Cited Document 1, to predict that 'the position of the half value in the layer is cooperative with other parameters, and there is an optimum relationship'".

(B) However, the position of the half value of the maximum concentration of the impurity atoms is as examined in A to C above.

As described above, the Appellant's allegation cannot be accepted.

E Summary

As described above, the Invention could have been easily made by a person skilled in the art, based on the Cited Invention and the technical matters described in Cited Document 1.

No. 4 Closing

As described above, the description of the scope of claims of the present application does meet the requirements stipulated in Article 36(6)(ii) of the Patent Act, and Article 36(6)(i) of the Patent Act. Further, the Invention could have been easily made by a person ordinarily skilled in the field of the art, to which the invention belongs, prior to the application, based on the Cited Invention and the technical matters described in Cited Document 1, and thus the Appellant should not be granted a patent under the provisions of Article 29(2) of the Patent Act.

Therefore, the present application should be rejected without examining inventions relating to other claims.

Therefore, the appeal decision shall be made as described in the conclusion.

January 22, 2021

Chief administrative judge: YAMAMURA, Hiroshi
Administrative judge: NOMURA, Nobuo
Administrative judge: YOSHINO, Mihiro