Appeal Decision

Appeal No. 2020-10043

Appellant Qualcomm, Inc.

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The case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2016-546024, entitled "SWITCHABLE ANTENNA ARRAY" [International Publication No. WO 2015/108644 published on July 23, 2015, National Publication of International Patent Application No. 2017-510130 published on April 6, 2017] has resulted in the following appeal decision.

Conclusion

The appeal of the case was groundless.

Reason

1. History of the procedures

The present application was filed on December 15, 2014 as an international filing date (priority claim under the Paris Convention received by the foreign receiving office on January 17, 2014, United States, and on December 12, 2014, United States). A written amendment was submitted on November 28, 2017. A notice of reasons for refusal was issued on November 29, 2018. A written amendment was submitted on March 4, 2019. A notice of reasons for refusal was issued on August 7, 2019. A written amendment was submitted on December 16, 2019. An examiner's decision of refusal was issued on April 24, 2020. An appeal against the examiner's decision of refusal was made on July 17, 2020, and a written amendment was submitted at the same time.

2. The Invention

The invention according to Claim 1 of the present application (hereinafter referred to as "the Invention") is recognized as follows specified by the matters recited in Claim 1 of the scope of claims in the written amendment submitted on July 17, 2020.

"An apparatus comprising:

an impedance circuit; and

a plurality of inductors coupled to the impedance circuit, each of the plurality of inductors being coupled in parallel to a corresponding switch of a plurality of switches, wherein

an input part of the corresponding switch of each of the inductors is coupled to a common node, which is an output part of the impedance circuit, and

the impedance circuit includes a matching network."

3. Reasons for refusal stated in the examiner's decision

The reasons for refusal stated in the examiner's decision is as follows: The invention according to Claim 1 of this application could have been easily made by a person ordinarily skilled in the art of the invention before the priority date of the present application (hereinafter referred to as "Priority date"), on the basis of the invention described in the following Cited Document 1 which was distributed or made publicly available through an electric telecommunication line in Japan or a foreign country, prior to the Priority date. Thus, the Appellant should not be granted a patent for the invention under the provisions of Article 29(2) of the Patent Act.

Cited Document 1: Japanese Unexamined Patent Application Publication No. 2003-338773

4. Cited documents

(1) Cited Document 1

Japanese Unexamined Patent Application Publication No. 2003-338773 (hereinafter referred to as "Cited Document 1", the underlines were added by the body) published on November 28, 2003, which is before the Priority date of the application, cited in the reasons for refusal stated in the examiner's decision, includes the following matters.

"[Claim 1] A high-frequency switching circuit of an SPDT type comprising first, second, and third input/output terminals and a connection point between a first signal path passing through the first input/output terminal and a second signal path passing through the second input/output terminal, and formed by serially connecting a first circuit including a switching element to the first signal path, serially connecting a second circuit including a switching element to the second signal path, and connecting the connection point to the third input/output terminal, wherein each of the first and second circuits includes a parallel circuit formed of a switching element and an inductor,
and an impedance element including a capacitance component is connected between the connection point and the ground so that input/output VSWR may be reduced in accordance with an impedance component to be generated by a wire or a strip line between the first and second input/output terminals and input/output sections of the first and second circuits, and an impedance component generated by wire or a strip line between the third input/output terminal and the connection point."

"[0015]
[Embodiments of the invention] The configuration of a high-frequency switching circuit according to the first embodiment is illustrated in FIG. 1 to FIG. 4. FIG. 1 is a circuit diagram of the high-frequency switching circuit. 11 is a first input/output terminal, 12 is a second input/output terminal, 13 is a third input/output terminal, and 14 is a connection point. As is the case with the example shown in FIG. 11, the first circuit is configured by a parallel circuit formed of a switching element 21 and an inductor 31, and the second circuit is configured by a parallel circuit formed of a switching element 22 and an inductor 32. The first circuit 1 is serially connected to a first signal path between the first input/output terminal 11 and the connection point 14, and the second circuit 2 is serially connected to a second signal path between the second input/output terminal 12 and the connection point 14.
[0016] FIG. 2 illustrates a concrete circuit of the switching element 21 and the vicinity thereof. The switching element 21 is formed of an FET having a drain and a source between which the inductor 31 is connected. A gate signal is applied to a gate via a resistor R. When the FET is ON, drain-source voltage is equivalent to a low-impedance resistance element, or when the FET is OFF, the drain-source voltage is equivalent to a capacitance element. The same applies to the switching element 22.
[0017] Returning to FIG. 1, 41 is an impedance component generated between the first circuit 1 and the first input/output terminal 11, and 42 is an impedance component

generated between the second circuit 2 and the second input/output terminal 12. The impedance components 41, 42 are impedance components generated by wires or strip lines arranged between the first and second input/output terminals 11, 12 and the input/output sections of the first and second circuits 1, 2. 43 is an impedance component generated between the third input/output terminal 13 and the connection point 14, which is an impedance component generated by a wire or a strip line which serves as a path between the third input/output terminal 13 and the connection point 14. The impedance components 41, 42 and 43 are formed mainly of inductance components, respectively.

[0018] 74 is an impedance element connected between the connection point 14 and the ground. 54 is a capacitance component, 64 is an inductance component thereof. Actually, a capacitor (capacitance element) is connected between the connection point 14 and the ground. The inductance component 64 corresponds to an inductance component of a wire or a strip line for connecting them.

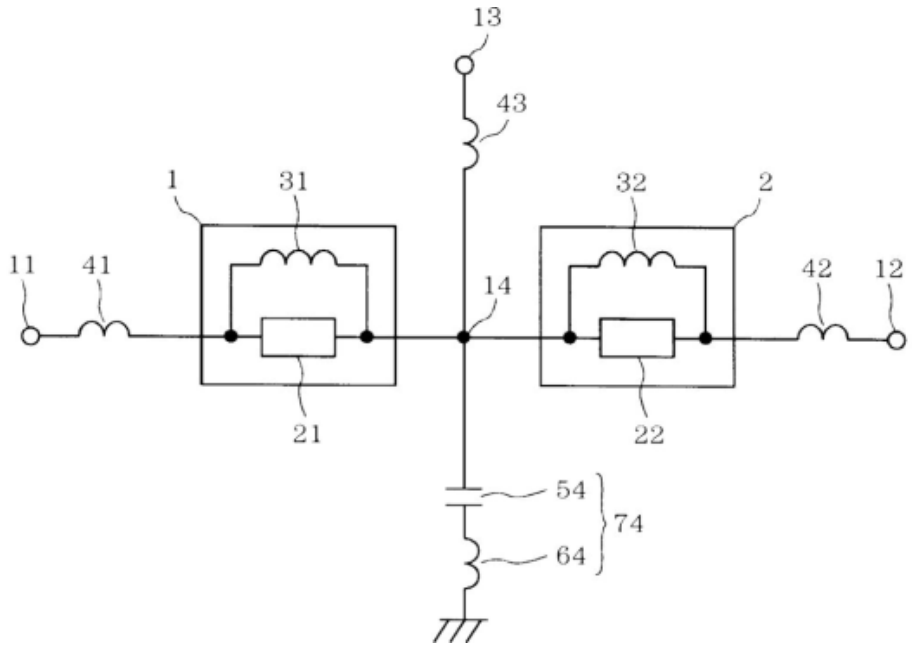
[0019] The high-frequency switching circuit shown in FIG. 1 operates as follows. When a signal passes from the first input/output terminal 11 to the third input/output terminal 13, the switching element 21 is equivalent to a simple resistance element, and the switching element 22 is equivalent to a simple capacitive element. Isolation must be required between the first input/output terminal 11 and the second input/output terminal 12 and between the second input/output terminal 12 and the third input/output terminal 13. Accordingly, an inductor 32 is connected in parallel to the switching element 22, to configure a parallel resonance circuit by the capacitance component of the switching element 22 in OFF state and the inductance component of the inductor 32. The inductance of the inductor 32 is defined so that a resonance frequency of the parallel resonance circuit is equal to a signal frequency to be input from the first input/output terminal 11. Leakage of signals to the second input/output terminal 12 can be prevented, accordingly.

[0020] Also when a signal passes from the second input/output terminal 12 to the third input/output terminal 13, in the same way, a parallel resonance circuit is configured by the capacitance component of the switching element 21 in OFF state and the inductance component of the inductor 31. The inductance of the inductor 31 is defined so that a resonance frequency of the parallel resonance circuit is equal to a signal frequency to be input from the second input/output terminal 12. Leakage of signals to the first input/output terminal 11 can be prevented, accordingly.

[0021] However, as an input frequency increases, the influence of the inductance components of the impedance components 41, 42, 43 increases. Thus, the input/output

VSWR is degraded and signals are not efficiently input/output, thereby degrading insertion loss. In this example, the problem is solved by connecting the impedance element 74 between the connection point 14 and the ground."

"[FIG. 1]



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In light of the above, Cited Document 1 describes the following invention (hereinafter referred to as "Cited Invention").

"A high-frequency switching circuit of an SPDT type comprising first, second, and third input/output terminals and a connection point between a first signal path passing through the first input/output terminal and a second signal path passing through the second input/output terminal, and formed by serially connecting a first circuit including a switching element to the first signal path, serially connecting a second circuit including a switching element to the second signal path, and connecting the connection point to the third input/output terminal, wherein

an impedance element including a capacitance component is connected between the connection point and the ground so that input/output VSWR may be reduced,

the first circuit is configured by a parallel circuit formed of a switching element 21 and an inductor 31, and the second circuit is configured by a parallel circuit formed of a switching element 22 and an inductor 32, the first circuit 1 is serially connected to

the first signal path between the first input/output terminal 11 and the connection point 14, and the second circuit 2 is serially connected to the second signal path between the second input/output terminal 12 and the connection point 14,

regarding a concrete circuit of the switching element 21 and the vicinity thereof, the switching element 21 is formed of a FET having a drain and a source between which the inductor 31 is connected,

an impedance component 43 generated between the third input/output terminal 13 and the connection point 14 is an impedance component generated by a wire or a strip line which serves as a path between the third input/output terminal 13 and the connection point 14,

an impedance element 74 connected between the connection point 14 and the ground is formed of a capacitance component 54 and an inductance component 64 thereof, actually, a capacitor (capacitance element) is connected between the connection point 14 and the ground, the inductance component 64 corresponds to an inductance component of a wire or a strip line for connecting them,

as an input frequency increases, the influence of the inductance components of the impedance components 41, 42, 43 increases, thus, the input/output VSWR is degraded and signals are not efficiently input/output, thereby degrading insertion loss, the problem is solved by connecting the impedance element 74 between the connection point 14 and the ground,

to allow signals to pass from the first input/output terminal 11 to the third input/output terminal 13, or to allow signals to pass from the second input/output terminal 12 to the third input/output terminal 13."

(2) Cited Document 2 and Cited Document 3

International publication No. 2009/022654 (hereinafter referred to as "Cited Document 2", the underlines were added by the body) published on February 19, 2009, which is before the Priority date of the present application, includes the following matters.

"[0003] FIG. 1 shows a switch circuit of the background art that uses FETs, this FIG. 1 being a circuit diagram showing the configuration of a SPDT (Single-Pole Double-Through) switch circuit."

"[0014] In the switch circuit shown in FIG. 1, the input of a high-level or a low-level

control signal to a control terminal 11 provided in a first switch unit 21 and a control terminal 12 provided in a second switch unit 22 controls the ON/OFF of the first switch unit 21 and the second switch unit 22. If complementary input of high-level and low-level binary control signals is applied to the control terminal 11 and the control terminal 12 at this time, the high-frequency signal that was applied as input from the first high-frequency terminal 1 can be supplied as output from the second high-frequency terminal 2 or the third high-frequency terminal 3, and one of the high-frequency signals applied as input from the second high-frequency terminal 2 and the third high-frequency terminal 3 can be supplied as output from the first high-frequency terminal 1."

International publication No. 2007/136050 (hereinafter referred to as "Cited Document 3", the underlines were added by the body) published on November 29, 2007, which is before the Priority date of the present application, includes the following matters.

"[0004] FIG. 1 is an example of a high-frequency switch circuit using FETs, a circuit diagram showing a high-frequency switch circuit configuration of an SPDT (single pole double through) type. Here, FIG. 2 is a circuit disposed in FIG. 1 of Japanese Unexamined Patent Application Publication No. H08-139014.
[0005] The high-frequency switch circuit shown in FIG. 1 has a configuration including a first switch section 121 and a second switch section 122 for allowing a high-frequency signal to pass through or for cutting off a high-frequency signal.
[0006] The first switch section 121 includes a plurality of FETs (four in FIG. 1) connected in series with its two ends connected to two high-frequency terminals 101 and 102. The gate terminal of each FET is connected to a control terminal 111 via a resistance element. Similarly, the second switch section 122 includes a plurality of FETs (four in FIG. 1) connected in series with its two ends connected to two high-frequency terminals 101 and 103. The gate terminal of each FET is connected to a control terminal 112 via a resistance element. Here, the high-frequency terminal 101 is shared by the first switch section 121 and the second switch section 122.
[0007] In the high-frequency switch circuit shown in FIG. 1, a high-level or low-level control signal is input to the control terminal 111 of the first switch section 121 and the control terminal 112 of the second switch section 122 so as to perform on/off control of the first switch section 121 and the second switch section 122. In this configuration, when two levels of control signals, high-level and low-level signals, are complementarily input to the control terminal 111 and the control terminal 112, it is

possible to cause the high-frequency terminal 102 or the high-frequency terminal 103 to output the high-frequency signal input from the high-frequency terminal 101, or the cause high-frequency terminal 101 to output one of the high-frequency signals input from the high-frequency terminal 102 and the high-frequency terminal 103."

According to the Cited Documents 2 and 3, the following matter is considered to be well-known.
"In a circuit diagram showing the configuration of an SPDT switch circuit, controlling ON/OFF of first and second switch circuits allows a high-frequency signal input from a first high-frequency terminal to be output from a second or third high-frequency terminal or allows one of high-frequency signals input from the second and third high-frequency terminals to be output from the first high-frequency terminal." (hereinafter referred to as "Well-known art 1")

(3) Cited Document 4 and Cited Document 5

The microfilm of Japanese Utility Model Application No. H3-30588 (Japanese Unexamined Utility Model Application Publication No. H4-126403) (hereinafter referred to as "Cited Document 4", the underlines were added by the body) published on November 18, 1992, which is before the Priority date of the present application, includes the following matters.

"[0021] [Advantage of the device] As described above, this device is configured to arrange a cross polarization absorption member adjacent to one end of a member rotating a polarization plane embedded in a dielectric rod so as to suppress a cross polarization component immediately after the polarization plane is rotated by the member rotating the polarization plane, thereby improving matching characteristics (variation in VSWR or characteristic impedance) between the dielectric rod and a waveguide, resulting in reducing transmission loss, accordingly.

Japanese Unexamined Patent Application Publication No. 2000-201015 (hereinafter referred to as "Cited Document 5", the underlines were added by the body) published on July 18, 2020, which is before the Priority date of the present application, includes the following matters.

"[0006] However, the coaxial resonant slot antenna, which is configured by bonding an

insulating substrate 501a with a slot 503 to an insulating substrate 501b with a band-like conductive layer 504, is likely to cause variation in electro-magnetic connection due to relative displacement between the slot 503 and the band-like conductive layer 504 generated by the bonding, and may cause significant variability of resonance frequency or VSWR (Voltage Standing Wave Ratio) indicating impedance matching state. For reducing the variability of VSWR, the insulating substrate 501a, 501b, the slot 503, and the band-like conductive layer 504 must be precisely formed, and accurate bonding between the insulating substrates 501a, 501b is required, which complicates a manufacturing process."

According to the Cited Documents 4 and 5, the following matter is considered to be well known.
"VSWR indicates impedance matching state" (hereinafter referred to as "Well-known art 2")

5. Comparison between the Invention and the Cited Invention

The "connection point 14" in the Cited Invention corresponds to the "common node" in the Invention.

The "impedance element 74" in the Cited Invention is "connected between the connection point 14 and the ground", and the "impedance component 43" is generated "between the third input/output terminal 13 and the connection point 14". Thus, it can be said that the "impedance element 74" and the "impedance component 43" form an "impedance circuit" as a whole.

Taking into consideration that "an impedance element including a capacitance component is connected between the connection point and the ground so that input/output VSWR may be reduced", or "an impedance element 74 is connected between the connection point 14 and the ground" in order to solve the problem that "the input/output VSWR is degraded and signals are not efficiently input/output, thereby degrading insertion loss", and that the matter "the VSWR indicates impedance matching state" is well known as indicated as Well-known art 2, the "impedance element 74" is an element that eliminates degradation of impedance matching, and it can be said that the "impedance element 74" and the "impedance component 43" "includes a matching network" connected to the third input/output terminal and the connection point 14.

The "first circuit" in the Cited Invention is a parallel circuit of the switching element 21 and the inductor 31, specifically, the "inductor 31" is connected between the drain and the source of the FET being the switching element 21. The "second circuit" is also a parallel circuit of the switching element 22 and the inductor 32. Thus, it can be said that "each of a plurality of inductors is coupled in parallel to a plurality of switches".

The parallel circuit of the switching element 21 and the inductor 31 constitutes the first circuit 1, and the parallel circuit of the switching element 22 and the inductor 32 constitutes the second circuit 2 to be connected to the connection point 14. A "matching network" formed of the "impedance element 74" and the "impedance component 43" is connected to the connection point 14. Thus, it can be said that the "inductor 31" and the "inductor 32" are "coupled to the impedance circuit", that "each of the plurality of inductors is coupled in parallel to a corresponding switch of a plurality of switches", and that "the corresponding switch of each of the inductors is coupled to a common node".

Therefore, the Invention and the Cited Invention have the following corresponding feature.

"An apparatus comprising:

an impedance circuit; and

a plurality of inductors coupled to the impedance circuit, each of the plurality of inductors being coupled in parallel to a corresponding switch of a plurality of switches, wherein

the corresponding switch of each of the inductors is coupled to a common node,

the impedance circuit includes a matching network."

The Invention and the Cited Invention have the following different feature.

(Different Feature)

Regarding a coupling between the corresponding switch of each of the inductors and the common node, the Invention is configured so that "an input part of the corresponding switch of each of the inductors is coupled to a common node, which is an output part of the impedance circuit", while the Cited Invention only describes a case of allowing signals to pass from the first input/output terminal 11 to the third input/output terminal 13 and a case of allowing signals to pass from the second input/output terminal

12 to the third input/output terminal 13, although the corresponding switch of each of the inductors is coupled to a common node, or only describes a case where "an output part of the corresponding switch of each of the inductors is coupled to a common node, which is an input part of the impedance circuit". (In other words, the Invention discloses signals from the impedance circuit to the inductors, while the Cited invention discloses signals from the first or second circuit to the "matching network" formed of "the impedance element 74 and the impedance component 43". The Invention and the Cited Invention are different in direction of the signals.)

6. Judgment by the body

The Different Feature is examined below.

In the Cited Invention, all of the "first input/output terminal", the "second input/output terminal", and the "third input/output terminal" are terminals to perform "input and output". It is obvious that these terminals can be used both for inputting and outputting signals.

Thus, even though the Cited Invention only describes a case of allowing signals to pass from the first input/output terminal 11 to the third input/output terminal 13 and a case of allowing signals to pass from the second input/output terminal 12 to the third input/output terminal 13, or a case where the first and second terminals 11 and 12 are used only for input and the third terminal 13 is used only for output, it is obvious that signals can be input from the third terminal 13 and output from the first terminal 11 or the second terminal 12.

In addition, as indicated in Well-known art 1, in a high-frequency switching circuit of an SPDT type, controlling ON/OFF of first and second switch circuits allows a high-frequency signal input from a first high-frequency terminal to be output from a second or third high-frequency terminal or allows one of high-frequency signals input from the second and third high-frequency terminals to be output from the first high-frequency terminal, and this is well known. Therefore, it is also obvious from Well-known art 1 that the Cited Invention allows signals to pass from the third input/output terminal 13 to the first input/output terminal 11 and allows signals to pass from the third input/output terminal 13 to the second input/output terminal 12.

The case in the Cited Invention allowing signals to pass from the third

input/output terminal 13 to the first input/output terminal 11 or the second input/output terminal 12 indicates that "an input part of the corresponding switch of each of the inductors is coupled to a common node, which is an output part of the impedance circuit formed of an impedance element 74 and an impedance component 43".

The effect of the Invention configured as above falls within a scope that can be predicted based on the Cited Invention and well-known arts.

Thus, the Invention could be easily made based on the Cited Invention.

7. Closing

As above, the Invention could be easily made by a person skilled in the art based on the Cited Invention. The Appellant should not be granted a patent for the invention under the provisions of Article 29(2) of the Patent Act.

The present application should be rejected without examining the inventions according to other claims.

Therefore, the appeal decision shall be made as described in the conclusion.

March 18, 2021

Chief administrative judge: SATO, Tomoyasu
Administrative judge: YOSHIDA, Takayuki
Administrative judge: TANIOKA, Yoshihiko