Appeal Decision

Appeal No. 2020-13425

Appellant Dexerials Corporation

Patent Attorney Tajime International Patent Firm

The case of appeal against the examiner's decision of refusal of Japanese Patent Application No. 2016-4538, entitled "Multilayer Substrate" (the application published on July 21, 2016, Japanese Unexamined Patent Application Publication No. 2016-131245) has resulted in the following appeal decision.

Conclusion

The appeal of the case was groundless.

Reason

No. 1 History of the procedures

The present application was filed on January 13, 2016 (Priority Claim: January 13, 2015 Japan (JP)), and the outline of history of the procedures is as follows.

January 9, 2019	: Submission of written amendment
Dated September 26, 2019	: Notice of reasons for refusal
January 28, 2020	: Submission of written opinion and written amendment
Dated June 23, 2020	: Examiner's decision of refusal
September 25, 2020	: Submission of written demand for appeal and written amendment
October 30, 2020	: Submission of written amendment (formality)

No. 2 Decision to dismiss amendment on the written amendment dated September 25, 2020

[Conclusion of Decision to Dismiss Amendment]

The amendment dated September 25, 2020 shall be dismissed.

[Reason]

1 Outline of amendment

The written amendment dated September 25, 2020 (hereinafter, referred to as "the Amendment") includes an amendment which amends the invention of

"A multilayer substrate comprising semiconductor substrates which each have a through electrode and are laminated to each other, wherein

conductive particles are each regularly disposed and at least conductive particles are present at a position where the through electrodes face each other as viewed in a plan view of the multilayer substrate, and

the multilayer substrate has a connection structure in which the facing through electrodes are connected by the conductive particles, and the semiconductor substrates each having the through electrode are bonded together by an insulating adhesive" (hereinafter, referred to as "the Invention") which is specified by the matter specifying the invention described in Claim 1 of the scope of claims amended on January 28, 2020, to

the invention of "A multilayer substrate comprising semiconductor substrates which each have a through electrode and are laminated to each other on a wiring board or a semiconductor substrate having a through electrode, wherein

conductive particles are each regularly disposed and at least conductive particles are present at a position where the through electrodes face each other as viewed in a plan view of the multilayer substrate,

between the substrates configuring the multilayer substrate, the number of conductive particles which are not captured by the facing through electrodes is 5% or less, relative to the total number of the conductive particles, and

the multilayer substrate has a connection structure in which the facing through electrodes are connected by the conductive particles, and the semiconductor substrates each having the through electrode are bonded together by an insulating adhesive" (hereinafter, referred to as "the Amended Invention"). Further, the underlined portions indicate the amended portions.

2 Propriety of amendment

The Amendment according to Claim 1 is a correction that restricts the place where "semiconductor substrates which each have a through electrode" are laminated to "on a wiring board or a semiconductor substrate having a through electrode," and further restricts the number of "conductive particles" to "between the substrates

configuring the multilayer substrate, the number of conductive particles which are not captured by the facing through electrodes is 5% or less, relative to the total number of the conductive particles," and the invention described in Claim 1 before the Amendment and the invention described in Claim 1 after the Amendment are identical in field of industrial application and the problem to be solved. Therefore, the Amendment aims at the restriction of the scope of claims stipulated in Article 17-2(5)(ii) of the Patent Act.

In addition, there is no matter that violates Article 17-2(iii) and (iv) of the Patent Act.

Then, it will be examined below whether or not the invention described in Claim 1 by the Amendment (hereinafter, referred to as "the Amended Invention") falls under the provisions of Article 126(7) of the Patent Act which is applied mutatis mutandis pursuant to the provisions of Article 17-2(6) of the Patent Act (whether or not the Appellant can be granted a patent independently at the time of filing of the patent application).

(1) The Amended Invention

The Amended Invention is as described in "1" above.

(2) Described matters in the Cited Documents

A Cited Document 1

(A) Japanese Unexamined Patent Application Publication No. 2002-110897 (hereinafter, referred to as "Cited Document 1") cited in the reasons for refusal stated in the examiner's decision describes the following together with drawings.

a "[0020] (First Embodiment) FIG. 1 is a cross-sectional view showing <u>a multi-chip semiconductor device</u> according to the first embodiment of the present invention. In FIG. 1, <u>a plurality of semiconductor chips 2a and 2b</u> are laminated on a wiring board 1 with anisotropic conductive films 3a and 3b interposed therebetween. <u>The semiconductor chips 2a and 2b are electrically connected to each other by plugs 4a and 4b made of Cu or Al embedded in through holes, and bumps 5a and 5b integrally provided on the plugs 4a and 4b</u>.

[0021] That is, the semiconductor chips 2a and 2b are provided with a plurality of semiconductor elements 6a and 6b (only one is shown for each chip in the figure), and these semiconductor elements 6a and 6b are connected to the bumps 5a and 5b via a Cu/TaN layer 7, whereby the plurality of semiconductor elements 6a and 6b of the semiconductor chips 2a and 2b are electrically connected to each other.

[0022] The electrical connection between an electrode 8 of the wiring board 1 and the plug 4a and the electrical connection between the bump 5a and the plug 4b are realized by anisotropic conductive films 3a and 3b which are normally insulating, but become conductive when pressure is applied. By using the anisotropic conductive films, it is possible to omit the step of forming an insulating film on the back surface of the chips to be laminated.

[0023] Next, a method of manufacturing the multi-chip semiconductor device configured as described above will be described with reference to FIG. 2.

[0024] As shown in FIG. 2 (a), a resist pattern 11 is formed on the upper surface of the silicon substrate 10 on which the semiconductor element 6a is formed, the silicon substrate 10 is etched using the resist pattern 11 as a mask, and a chip contact hole 12 is formed on the silicon substrate 10.

[0025] Next, after peeling off the resist pattern 11, as shown in FIG. 2 (b), an SiO2 film 13 is formed on the front surface including the inner surface of the chip contact hole 12. Then, the contact pattern for rewiring is exposed by lithography using a dry film and the like to form a mask pattern 14, and the SiO2 film 13 is etched by RIE and the like using this as a mask to form a contact hole 15 for connecting the semiconductor element 6a.

[0026] Next, after the resist pattern 14 is peeled off, as shown in FIG. 2 (c), a Cu/TaN layer 16 serving as a barrier metal and a seed layer is formed on the front surface including the inner surfaces of the holes 12 and the contact holes 15.

[0027] After that, as shown in FIG. 2 (d), a resist pattern 17 is formed in a region excluding the plug and bump forming regions, and the resist pattern 17 is used as a mask and metal is adhered by electrolytic plating to integrally form a plug 18 filling the hole 12 and the bump 19 connecting the semiconductor element 6a.

[0028] Since the metal to be adhered by electroplating may be subsequently formed with a polyimide film and the like, it is a metal having a melting point equal to or higher than the formation temperature of the polyimide film; that is, a metal having a melting point of 400°C. or higher. Specific examples of such a metal include Al, Cu, Au, Ag, and the like.

[0029] Next, as shown in FIG. 2 (e), the resist pattern 17 is peeled off, the exposed Cu/TaN layer 16 is removed by etching, and the back surface of the silicon substrate 10a is further polished until the plug 18 is exposed; that is, Si and the insulating film at the bottom of the through plug is removed with CMP, RIE, etc.

[0030] The semiconductor chip 2a thus obtained is disposed on the wiring board 1 via the anisotropic conductive film 3a, and the semiconductor chip 2b similarly produced is further disposed thereon via the anisotropic conductive film 3b, thereby obtaining a

multi-chip semiconductor device having the structure shown in FIG. 1. In this case, the number of semiconductor chips to be laminated can be 3 to 4 layers.
[0031] As described above, the electrical connection between the electrode 8 of the wiring board 1 and the plug 4a and the electrical connection between the bump 5a and the plug 4b are realized by anisotropic conductive films 3a and 3b in which conductive particles are dispersed in insulating material, and which are normally insulating, but become conductive when pressure is applied. Further, the chip and the chip can be electrically connected by other than the anisotropic conductive film, and can be connected by, for example, Cu bump and Sn plating, Au bump and Sn, solder, and the like.

b FIG. 1
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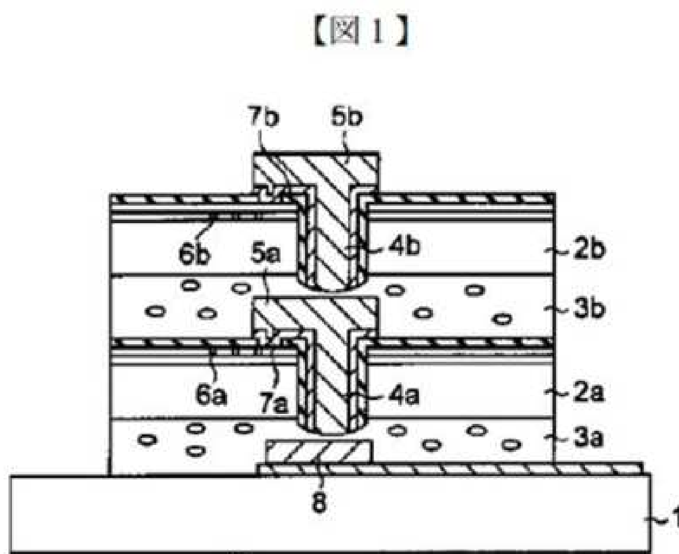

【図１】 [FIG. 1]

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(B) According to the above description and the drawings of Cited Document 1, the following matters are described.
a According to Paragraph [0020] of "(A) a," Cited Document 1 describes a multi-chip semiconductor device.

Then, according to Paragraph [0020] of "(A) a,", it can be said that in the multi-chip semiconductor device, a plurality of semiconductor chips 2a and 2b are laminated. Further, according to Paragraphs [0024] and [0030] of "(A) a," "semiconductor chips 2a

and 2b" are obtained by forming semiconductor elements on a silicon substrate.

Therefore, it can be said that Cited Document 1 describes a multi-chip semiconductor device in which a plurality of semiconductor chips 2a and 2b obtained by forming semiconductor elements on a silicon substrate are laminated.

b According to Paragraph [0020] of "(A) a," the semiconductor chips 2a and 2b are electrically connected to each other by plugs 4a and 4b embedded in through holes and bumps 5a and 5b integrally provided on the plugs 4a and 4b.

c According to Paragraph [0030] of "(A) a," the semiconductor chip 2b produced similarly to the semiconductor chip 2a is disposed on the semiconductor chip 2a via the anisotropic conductive film 3b, and the number of semiconductor chips to be laminated can be 3 to 4 layers.

d "According to FIG. 1 of "(A) b," it can be seen that the bump 5a integrally provided on the plug 4a formed in the semiconductor chip 2a, and the plug 4b formed in the semiconductor chip 2b are opposite to each other.

e According to Paragraph [0031] of "(A) a," the electrical connection between the bump 5a and the plug 4b is realized by an anisotropic conductive film 3b in which conductive particles are dispersed in insulating material.

(C) According to a to e above, Cited Document 1 describes the following invention (hereinafter, referred to as "the Cited Invention").

"A multi-chip semiconductor device in which a plurality of semiconductor chips 2a and 2b obtained by forming semiconductor elements on a silicon substrate are laminated, wherein

the semiconductor chips 2a and 2b are electrically connected to each other by plugs 4a and 4b embedded in through holes and bumps 5a and 5b integrally provided on the plugs 4a and 4b,

the semiconductor chip 2b produced similarly to the semiconductor chip 2a is disposed on the semiconductor chip 2a via the anisotropic conductive film 3b, and the number of semiconductor chips to be laminated can be 3 to 4 layers,

the bump 5a integrally provided on the plug 4a formed in the semiconductor chip 2a, and the plug 4b formed in the semiconductor chip 2b are opposite to each other, and

the electrical connection between the bump 5a and the plug 4b is realized by an anisotropic conductive film 3b in which conductive particles are dispersed in insulating material".

B Cited Document 2

(A) Japanese Unexamined Patent Application Publication No. H3-62411 (hereinafter, referred to as "Cited Document 2") cited in the reasons for refusal described in the examiner's decision describes the following matters.

a "[Industrial Application]

The present invention relates to a method of manufacturing an anisotropic conductive film, and more particularly, to an anisotropic conductive film selectively arranging conductive particles at desired positions, and enabling high density connection of IC implementation, etc." (Page 1, lower right column, line 17 to page 2, upper left column, line 2)

b "[Problem to be solved by the invention]

However, there is a problem that when an anisotropic conductive film is used for connecting an electrode in a liquid crystal display element, etc. and an external drive circuit, insulation between adjacent electrodes cannot be maintained at a connection density of 10 lines/mm or more, and in the method of connecting an IC chip, since the area of the connection portion is as fine as about 0.01 mm^2, the number of conductive particles contributing to connection becomes small and the connection resistance becomes large.

In view of such a problem of a prior art, the object of the present invention is to manufacture an anisotropic conductive film which can be used for connection with higher connection density and lower connection resistance in a method of manufacturing an anisotropic conductive film". (Page 2, upper left column, line 10 to upper right column, line 5)

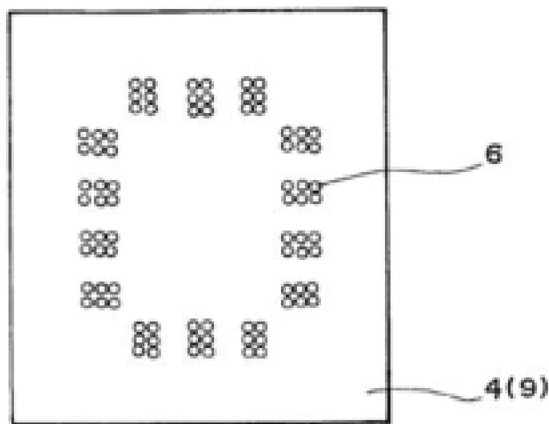
c "The anisotropic electric conduction films obtained in such a way selectively dispose conductive particles at desired positions (namely, usually positions corresponding to terminal portions to be connected by the anisotropic conductive films), and are used for high-density connection such as implementation of IC parts, as high density anisotropic conductive films of high connection resolution; that is, low resistance and high insulation". (Page 2, lower right column, lines 9 to 15)

d "FIG. 3 is a plan view showing an example of the anisotropic conductive film prepared as described above, and the conductive particles 6 are selectively sprayed on desired positions of the adhesive 4 or the insulating film 9.

The prepared anisotropic conductive film can be used for the implementation of an IC chip, for example, by aligning and mounting it on an IC implementation substrate, and after the IC chip is mounted thereon, heating and pressurizing it to function also as an adhesive". (Page 3, upper right column, line 17 to lower left column, line 5)

e FIG. 3

"



第 3 図

第３図 FIG. 3

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(B) Therefore, Cited Document 2 describes the following technology.

"In light of a problem that in the method of connecting an IC chip, since the area of the connection portion is fine, the number of conductive particles contributing to connection becomes small and the connection resistance becomes large, the anisotropic electric conduction films selectively dispose conductive particles at desired positions (namely, usually positions corresponding to terminal portions to be connected by the anisotropic conductive films), and the anisotropic conductive film is used for the

implementation of an IC chip by aligning and mounting it on an IC implementation substrate, and after the IC chip is mounted thereon, and making it to function also as an adhesive".

(3) Comparison with the Cited Invention

The Amended Invention and Cited Invention 1 will be compared.

A Since "a semiconductor chip 2a," and "a semiconductor chip 2b" of the Cited Invention are "obtained by forming semiconductor elements on a silicon substrate," the Cited Invention is equipped with a configuration corresponding to "semiconductor substrates" of the Amended Invention.

Then, in the Cited Invention, "the plug 4a" is formed in "the semiconductor chip 2a," "the plug 4b" is formed in "the semiconductor chip 2b," and "the semiconductor chips 2a and 2b" are "electrically connected to each other" by "plugs 4a and 4b embedded in through holes and bumps 5a and 5b integrally provided on the plugs 4a and 4b". Therefore, since "plugs 4a and 4b" are "embedded in through holes," it can be said that they are electrodes formed in the through holes.

Here, concerning "through electrodes" of the Amended Invention, since the specification of the present application [0030] describes that "the specifications of the through electrodes 4A, 4B, and 4C can be appropriately set. For example, the through electrodes 4A, 4B, and 4C may have an electrode pad or a bump," "through electrodes" of the Amended Invention include a through electrode equipped with a bump, and also include "plugs 4a and 4b and bumps 5a and 5b integrally provided on the plugs 4a and 4b" of the Cited Invention.

Furthermore, in the Cited Invention, "semiconductor chips 2a and 2b" "are laminated," and "the number of semiconductor chips to be laminated can be 3 to 4 layers".

Therefore, "a multi-chip semiconductor device" of the Cited Invention in which "a semiconductor chip 2a obtained by forming semiconductor elements on a silicon substrate" having "a plug 4a and a bump 5a integrally provide on the plug 4a," and "a semiconductor chip 2b obtained by forming semiconductor elements on a silicon substrate" having "a plug 4b and a bump 5b integrally provide on the plug 4b" are laminated corresponds to "a multilayer substrate comprising semiconductor substrates which each have a through electrode and are laminated to each other on a semiconductor substrate" of the Amended Invention.

Also, concerning "on a wiring board or a semiconductor substrate having a

through electrode" of the Amended Invention, the dependency between "having a through electrode" and "a semiconductor substrate" is unknown, and even if "a wiring board or a semiconductor substrate having a through electrode" is "a semiconductor substrate having a through electrode," in "a multi-chip semiconductor device" of the Cited Invention, "a semiconductor chip 2a obtained by forming semiconductor elements on a silicon substrate" having "a plug 4a and a bump 5a integrally provide on the plug 4a," and "a semiconductor chip 2b obtained by forming semiconductor elements on a silicon substrate" having "a plug 4b and a bump 5b integrally provide on the plug 4b" are laminated, so that it corresponds to "a multilayer substrate comprising semiconductor substrates which each have a through electrode and are laminated to each other on a semiconductor substrate having a through electrode " of the Amended Invention.

B In the Cited Invention, since "the bump 5a integrally provided on the plug 4a formed in the semiconductor chip 2a, and the plug 4b formed in the semiconductor chip 2b are opposite to each other," and "the electrical connection between the bump 5a and the plug 4b is realized by an anisotropic conductive film 3b in which conductive particles are dispersed in insulating material," it should be appreciated that "conductive particles" exist at the position where "the bump 5a" and "the plug 4" are opposite to each other.

Therefore, the fact that "conductive particles" are present at the position where "the bump 5a" and "the plug 4" are opposite to each other in the Cited Invention and the Amended Invention are common in that "at least conductive particles are present at a position where the through electrodes face each other as viewed in a plan view of the multilayer substrate".

However, they are different in that concerning conductive particles, in the Amended Invention, "conductive particles are each regularly disposed," and "between the substrates configuring the multilayer substrate, the number of conductive particles which are not captured by the facing through electrodes is 5% or less, relative to the total number of the conductive particles," whereas, that is not specified in Cited Invention.

C In the Cited Invention, since "the bump 5a integrally provided on the plug 4a formed in the semiconductor chip 2a, and the plug 4b formed in the semiconductor chip 2b are opposite to each other," and "the electrical connection between the bump 5a and the plug 4b is realized by an anisotropic conductive film 3b in which conductive

particles are dispersed in insulating material," it can be said that the Cited Invention also has a configuration in which "the bump 5a" and "the plug 4b" opposite to each other are electrically connected by "conductive particles," and it is common with "a connection structure in which the facing through electrodes are connected by the conductive particles" of the Amended Invention.

However, they are different in that concerning a connection structure, in the Amended Invention, "the semiconductor substrates each having the through electrode are bonded together by an insulating adhesive," whereas, that is not specified in Cited Invention.

Therefore, according to A to C, the Amended Invention and the Cited Invention are identical and different in the following features.

(Corresponding Feature)

"A multilayer substrate comprising semiconductor substrates which each have a through electrode and are laminated to each other on a semiconductor substrate, wherein
at least conductive particles are present at a position where the through electrodes face each other as viewed in a plan view of the multilayer substrate, and
the multilayer substrate has a connection structure in which the facing through electrodes are connected by the conductive particles".

(Different Feature 1)

Concerning conductive particles, in the Amended Invention, "conductive particles are each regularly disposed," and "between the substrates configuring the multilayer substrate, the number of conductive particles which are not captured by the facing through electrodes is 5% or less, relative to the total number of the conductive particles," whereas that is not specified in Cited Invention.

(Different Feature 2)

Concerning a connection structure, in the Amended Invention, "the semiconductor substrates each having the through electrode are bonded together by an insulating adhesive," whereas, that is not specified in the Cited Invention.

(4) Judgment on Different Features

A Regarding Different Feature 1

(A) As described in "(2) B" above, Cited Document 2 describes the technology that "In

light of a problem that in the method of connecting an IC chip, since the area of the connection portion is fine, the number of conductive particles contributing to connection becomes small and the connection resistance becomes large, the anisotropic electric conduction films selectively dispose conductive particles at desired positions (that is, usually positions corresponding to terminal portions to be connected by the anisotropic conductive films), and the anisotropic conductive film is used for the implementation of an IC chip by aligning and mounting it on an IC implementation substrate, and making it to function also as an adhesive after the IC chip is mounted thereon".

Further, in such a film electrically connecting a semiconductor chip component or a substrate and another substrate, the technology that disposes conductive particles at positions corresponding to electrodes by considering electric resistance between the electrode, is merely a conventional technology (if necessary, see page 2, upper left column, lines 3 to 15, page 2, upper right column, line 13 to lower left column, line 9, page 3, upper left column, lines 8 to 12, and FIG. 2 of Japanese Unexamined Patent Application Publication No. H3-30446, Paragraphs [0007], [0023], [0025], [0039], and [0045] of Japanese Unexamined Patent Application Publication No. 2002-75065, Paragraphs [0001], [0006], and [0011] to [0013] of Japanese Unexamined Patent Application Publication No. 2005-209454, and Paragraphs [0007], [0008], [0014], [0017], [0085] to [0088], [0114] to [0119], FIG. 3 and FIG. 10 of Japanese Unexamined Patent Application Publication No. 2009-191185), it is obvious that such a layout of the conductive particles is based on the rule of disposing them at positions corresponding to the electrodes to which they are connected.

(B) The Cited Invention and a conventional technology described in Cited Document 2 belong to a common technical field of conductive films for electrically connecting an electronic component to another electronic component.

In addition, since it is a matter of common general technical knowledge that when a semiconductor chip component or a substrate is connected to another substrate using an anisotropic conductive films in which conductive particles are dispersed, problems occur in electric resistance and the like between electrodes (if necessary, see page 2, lines 16 to 23 of International Publication No. WO00/34830, Paragraphs [0003] to [0005] of Japanese Unexamined Patent Application Publication No. H8-273440, and page 2, upper light column, line 11 to lower left column, line 8, and FIG. 7 of Japanese Unexamined Patent Application Publication No. S63-102110), even in the Cited Invention in which "the electrical connection between the bump 5a and the plug 4b is

realized by an anisotropic conductive film 3b in which conductive particles are dispersed in insulating material," it is merely a matter that could have naturally predicted by a person skilled in the art that problems may occur in electric resistance between "the bump 5a" and "the plug 4b".

Therefore, it could have been easily implemented by a person skilled in the art to apply the technology described in Cited Document 2 to "conductive particles" of the Cited Invention to regularly dispose the conductive particles.

(C) According to Paragraph [0022] of the description of the specification of the present application that "the conductive particles 11 which are each selectively disposed at a part where the through electrodes 4A and 4B face each other in this connection structure means that the conductive particles 11 are mainly present on facing surfaces of the through electrodes 4A and 4B or in the vicinity of the surfaces and one or more conductive particles 11 are captured on the facing surfaces of the through electrodes 4A and 4B," it is natural to understand that the matter of the Amended Invention that conductive particles are "not captured" means that conductive particles are not disposed on parts where through electrodes are opposite to each other.

Then, concerning "between the substrates configuring the multilayer substrate, the number of conductive particles which are not captured by the facing through electrodes is 5% or less, relative to the total number of the conductive particles" of the Amended Invention, in the specification of the present application, there are only descriptions that "although some conductive particles 11 may not be captured by the facing through electrodes 4A and 4B, the number of such conductive particles 11 is preferably 5% or less, and more preferably 0.5% or less, relative to the total number of the conductive particles present between the first semiconductor substrate 3A and the second semiconductor substrate 3B" (see Paragraph [0027]), and "the number of the conductive particles 11 which are not captured by the through electrodes 4A and 4B between the facing semiconductor substrates 3A and 3B after connection between the semiconductor substrates 3A and 3B using the anisotropic conductive film 10A or 10B is preferably 5% or less relative to the total number of the conductive particles 11 present between the facing semiconductor substrates 3A and 3B" (see Paragraph [0047]), and it is unclear whether or not there is a remarkable difference between the effect when the number of the conductive particles 11 not captured by the through electrodes 4A and 4B is 5% or less of the total number of the conductive particles 11 and the effect when the number exceeds 5%.

In addition, a disadvantageous specific example (comparative example) in which

"the number of the conductive particles not captured by the facing through electrodes exceeds 5% of the total number of the conductive particles" is not shown.

Therefore, no particular technical significance can be seen about a numerical value range of "between the substrates configuring the multilayer substrate, the number of conductive particles which are not captured by the facing through electrodes is 5% or less, relative to the total number of the conductive particles".

(D) The conventional technology described in Cited Document 2 mentioned in (A) above is a technology that selectively disposes conductive particles at positions corresponding to electrodes, and it is not assumed that conductive particles are disposed at positions other than electrodes, so that it could have been implemented appropriately by a person skilled in the art that when the conventional technology described in Cited Document 2 is adopted for the "conductive particles" of the Cited Invention, the number of the conductive particles other than that at a position between "the bump 5a" of "the semiconductor chip 2a" and "the plug 4b" of "the semiconductor chip 2b" is made to be 5% or less, relative to the total number of the conductive particles between "the semiconductor chip 2a" and "the semiconductor chip 2b".

(E) From the above, the configuration relating to Different Feature 1 could have been easily implemented by a person skilled in the art by applying the technology described in Cited Document 2 to the Cited Invention.

B Regarding Different Feature 2

According to the description of Paragraph [0031] of "(2)" "A" "(A)" above that " the electrical connection between the electrode 8 of the wiring board 1 and the electrical connection between the bump 5a and the plug 4b is realized by anisotropic conductive films 3a and 3b in which conductive particles are dispersed in insulating material,...," it can be said that "the anisotropic conductive film 3b" " between" "the semiconductor chips 2a and 2b" of the Cited Invention includes an insulating material.

Then, it is an ordinarily carried out matter that an insulating adhesive is used as an insulating material of an anisotropic conductive film (if necessary, see page 3, upper left column lines 1 to 17 of Cited Document 2, page 2, lower left column, lines 3 to 9 of Japanese Unexamined Patent Application Publication No. H3-30446, and Paragraph [0007] of Japanese Unexamined Patent Application Publication No. 2002-75065).

Therefore, a person skilled in the art could have easily conceived of the configuration relating to Different Feature 2 by adopting the insulating adhesive as the

insulating material of "the anisotropic conductive film 3b" of the Cited Invention.

C Appellant's allegation

(A) The Appellant, in the written amendment dated October 30, 2020, alleges that "FIG. 3 of Cited Document 3 is merely a schematic view, and cannot be said to properly represent the layout of the conductive particles in the anisotropic conductive film of Cited Document 3. This is because the anisotropic conductive film of FIG. 3 is manufactured as shown in FIG. 1 or FIG. 2 (page 2, lower right, lines 19 to page 3, lower left, line 5), and after all, the conductive particles are merely selectively dispersed in the desired positions on the adhesive 4 or the insulating film 9. That is, although the conductive particles are present in a region of the desired positions, they are not manufactured so as to be regularly disposed within the region, and rather it is understood that the conductive particles are randomly disposed within the region" (see page 2, lines 12 to 21).

However, concerning "conductive particles" of the Amended Invention, although it is described that "conductive particles are each regularly disposed and at least conductive particles are present at a position where the through electrodes face each other as viewed in a plan view of the multilayer substrate," there is no stipulation that they are to be "regularly disposed within the region," so that the Appellant's allegation cannot be said to be based of the scope of claims and cannot be accepted.

(B) Further, the Appellant, in the written amendment above, alleges that "the invention according to Claim 1 has a new feature that is not described or suggested in Cited Documents 2 and 3; that is, the matter 'between the substrates configuring the multilayer substrate, the number of conductive particles which are not captured by the facing through electrodes is 5% or less, relative to the total number of the conductive particles'. In addition, for the effect of the invention that 'simulation analysis of performance is facilitated, and the number of improvement step can be decreased' that can be obtained from the above-mentioned feature, Cited Documents 2 and 3 do not include description that would anticipate such an effect" (see page 2, lines 22 to 27)

However, according to the description "therefore, although some conductive particles 11 may not be captured by the facing through electrodes 4A and 4B, the number of such conductive particles 11 is preferably 5% or less, and more preferably 0.5% or less, relative to the total number of the conductive particles present between the first semiconductor substrate 3A and the second semiconductor substrate 3B. In particular, it is preferable that substantially all of the conductive particles 11 be captured

by the through electrodes 4A and 4B. This also applies to relations between other semiconductor substrates constituting the multilayer substrate 1A. When the number of conductive particles 11 which do not contribute to connection between the through electrodes 4A, 4B, and 4C is decreased, simulation analysis of performance is facilitated, and the number of improvement step can be decreased" of Paragraph [0027] of the specification of the present application, the effect of the invention that "simulation analysis of performance is facilitated, and the number of improvement steps can be decreased" can be obtained "when the number of conductive particles 11 which do not contribute to connection between the through electrodes 4A, 4B, and 4C is decreased," and it cannot be said that it can be obtained by setting the upper limit value of "5%," relative to "the total number of the conductive particles present between the first semiconductor substrate 3A and the second semiconductor substrate 3B" and decreasing the number of the conductive particles 11 not captured by the through electrodes 4A and 4B to 5% or less.

Further, there is no evidence that the effect "simulation analysis of performance is facilitated, and the number of improvement step can be decreased" can be obtained by decreasing the number of the conductive particles 11 not captured by the through electrodes 4A and 4B to "5%," relative to "the total number of the conductive particles present between the first semiconductor substrate 3A and the second semiconductor substrate 3B".

Therefore, the Appellant's allegation cannot be accepted.

D Consequently, the Amended Invention could have been easily invented by a person skilled in the art based on the invention described in Cited Document 1 and the technology described in Cited Document 2, and thus the Appellant should not be granted a patent independently at the time of filing of the patent application under the provision of Article 29(2) of the Patent Act.

3 Closing on the Amendment

Therefore, the Amendment violates the provisions of Article 126(7) of the Patent Act applied mutatis mutandis pursuant to Article 17-2(6) of the Patent Act, and thus shall be dismissed under the provisions of Article 53(1) of the Patent Act applied mutatis mutandis by replacing certain terms pursuant to Article 159(1) of the Patent Act.

Accordingly, decision has been made as described in the above-mentioned Conclusion of Decision to Dismiss Amendment.

No. 3 Regarding the Invention

1 The Invention

Since the written amendment dated September 25, 2020 was dismissed as described above, the inventions according to Claims 1 to 15 of the present application are as specified by the matters recited in Claims 1 to 15 of the scope of claims, which has been amended by the written amendment dated January 28, 2020, and the invention according to Claim 1 (the Invention) is as described in "No. 2" "[Reason]" "1" above, which is specified by the matter described in Claim 1.

2 Outline of reasons for refusal stated in the examiner's decision

The reasons for refusal stated in the examiner's decision are that the invention according to Claim 1 could have been easily invented by a person having ordinary skill in the art to which the inventions pertain based on the invention described in Japanese Unexamined Patent Application Publication No. 2002-110897 and the technology described in Japanese Unexamined Patent Application Publication No. H3-62411 distributed or available to public over an electric communication network before the filing of the application, and thus the Appellant should not be granted a patent for it under the provisions of Article 29(2) of the Patent Act.

3 Described matters in the Cited Documents

Japanese Unexamined Patent Application Publication No. 2002-110897 and Japanese Unexamined Patent Application Publication No. H3-62411 cited in the reasons for refusal stated in the examiner's decision correspond to "Cited Document 1" and "Cited Document 2" described in "No. 2 [Reasons] 2 (2)" above, and the described matters thereof are as described in "No. 2 [Reason] 2 (2) A (A)" and "No. 2 [Reason] 2 (2) B (A)" above.

Also, the invention described in Cited Document 1 (the Cited Invention) and the technology described in "Cited Document 2" are as mentioned in "No. 2 [Reason] 2 (2) A (C)" and "No. 2 [Reason] 2 (2) B (B)" above.

4 Comparison with the Cited Invention

The Invention corresponds to an invention made by deleting the limitation that a lamination place of "semiconductors which each have through electrodes" is "on a wiring board or a semiconductor substrate having a through electrode" and the limitation that the number of "conductive particles" is "between the substrates configuring the multilayer substrate, the number of conductive particles which are not

captured by the facing through electrodes is 5% or less, relative to the total number of the conductive particles" from the Amended Invention examined in "No. 2 [Reason] 2" above.

Therefore, in light of points described in "No. 2 [Reason] 2 (3)" above, the Invention and the Cited Invention are identical or different in the following features.

(Corresponding Feature)
"A multilayer substrate comprising semiconductor substrates which each have a through electrode and are laminated to each other, wherein
at least conductive particles are present at a position where the through electrodes face each other as viewed in a plan view of the multilayer substrate, and
the multilayer substrate has a connection structure in which the facing through electrodes are connected by the conductive particles".

(Different Feature 1)
Concerning conductive particles, in the Invention, "conductive particles are each regularly disposed," whereas that is not specified in Cited Invention.

(Different Feature 2)
Concerning the connection structure, in the Invention, "the semiconductor substrates each having the through electrode are bonded together by an insulating adhesive," whereas that is not specified in Cited Invention.

5 Judgment on Different Features
(1) Regarding Different Feature 1
As described in "No. 2 [Reason] 2 (4) A" above, a person skilled in the art could have easily conceived of the configuration relating to Different Feature 1 by applying a technology that "selectively disposes conductive particles at positions corresponding to terminal portion to be connected" described in Cited Document 2 to "conductive particles" of the Cited Invention.

(2) Regarding Different Feature 2
As described in "No. 2 [Reason] 2 (4) B" above, a person skilled in the art could have easily conceived of the configuration relating to Different Feature 2 by adopting an insulating adhesive as an insulating material of "the anisotropic conductive film 3b" of the Cited Invention.

No. 4 Closing

As described above, since the Appellant should not be granted a patent for the invention according to Claim 1 of the present application under the provisions of Article 29(2) of the Patent Act, the present application should be rejected without examining inventions relating to other claims.

May 31, 2021

Chief administrative judge: SAKAI, Tomohiro
Administrative judge: HATANAKA, Hiroyuki
Administrative judge: SUHARA, Hiromitsu